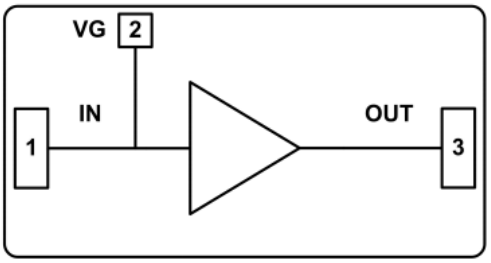
V1.0.0

GaAs pHEMT MMIC
Driver Amplifier
DC-6GHz

Features

- **Frequency: DC-6GHz**
- **Gain: 21dB**
- **Noise Figure: 1.0dB**
- **P1dB: +28 dBm @ VDD=+10V**
- **Psat: +29 dBm @ VDD=+10V**
- **Power Supply: +5/+8/+10 V @ 125 mA**
- **Input/Output: 50Ω**
- **Die Size: 1.0 × 0.67 × 0.1mm**

Functional Block Diagram



Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

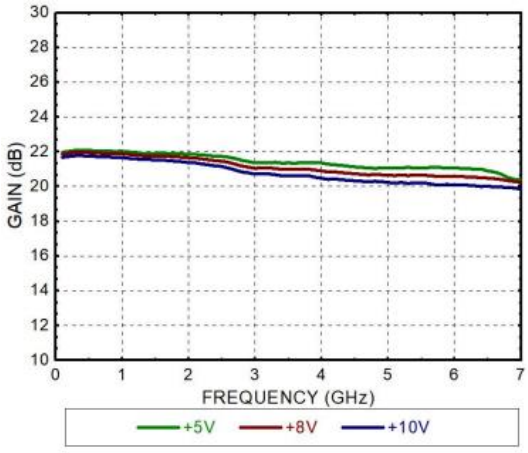
Electrical Specifications

TA = +25ºC, IDD = 125mA*

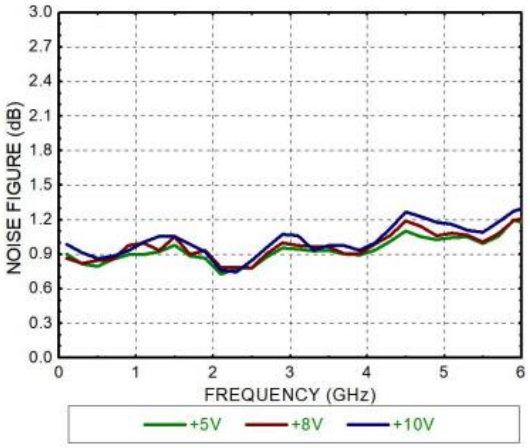
Parameters	VDD=+5V			VDD=+8V			VDD=+10V			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	DC-6			DC-6			DC-6			GHz
Gain		21			21			21		dB
Noise Figure		1.0			1.0			1.0		dB
Gain Flatness		±0.3			±0.4			±0.4		dB
P1dB		22.5			26.5			28		dBm
Psat		23.5			27.5			29		dBm
OIP3		35			39			40.5		dBm
Input Return Loss		15			15			15		dB
Output Return Loss		15			15			15		dB
Operating Current		125			125			125		mA

*The operating current can be controlled around 125mA by adjusting the VG voltage, and the VG regulation range: -0.8V ~ -0.2V.

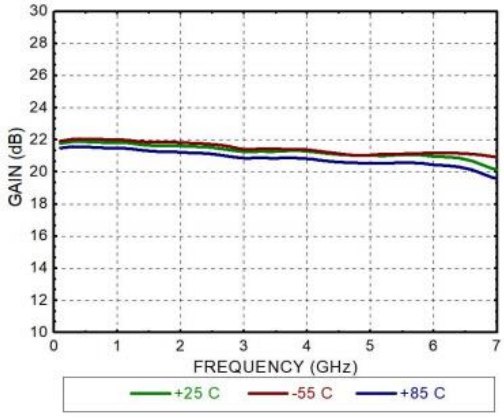
Gain vs. VDD



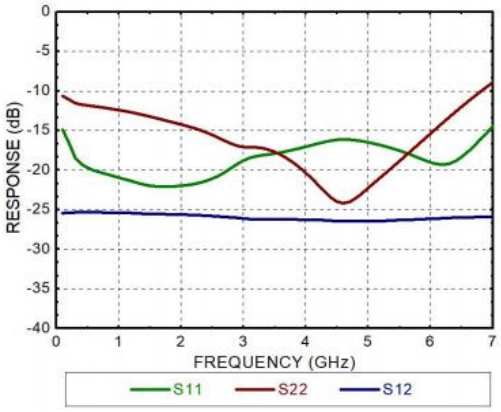
Noise Figure vs. VDD



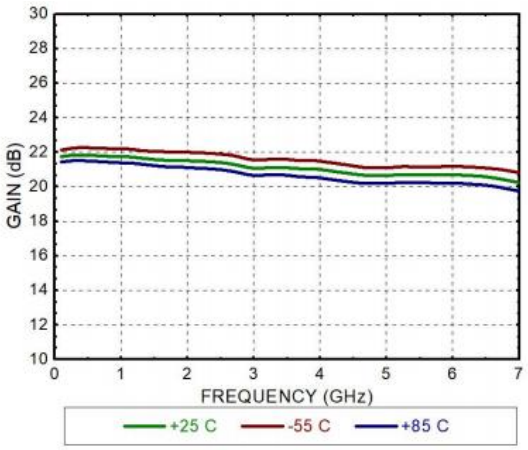
Gain vs. Temperature VDD=+5v



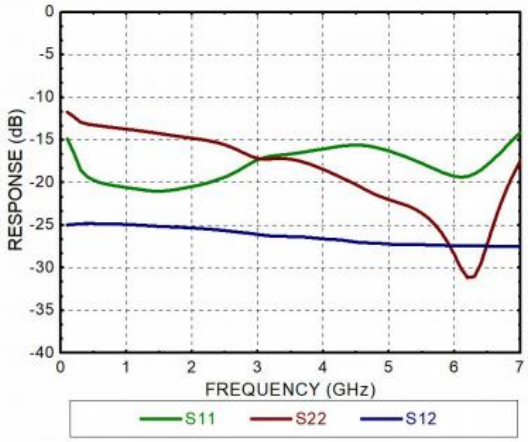
Return Loss&Reverse Isolation VDD=+5v



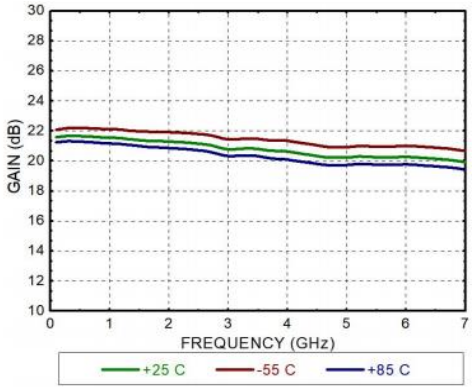
Gain vs. Temperature VDD=+8v



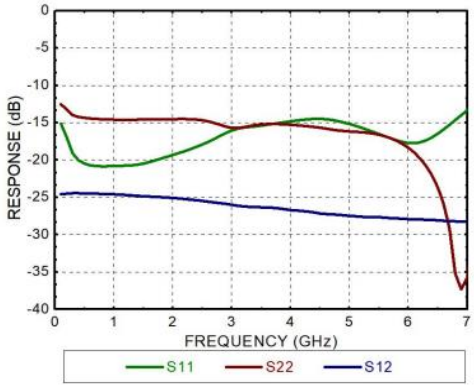
Return Loss&Reverse Isolation VDD=+8v



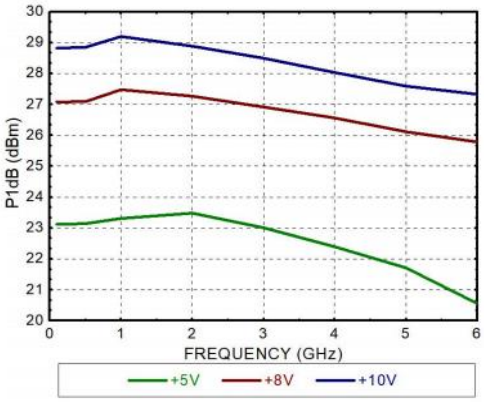
Gain vs. Temperature VDD=+10v



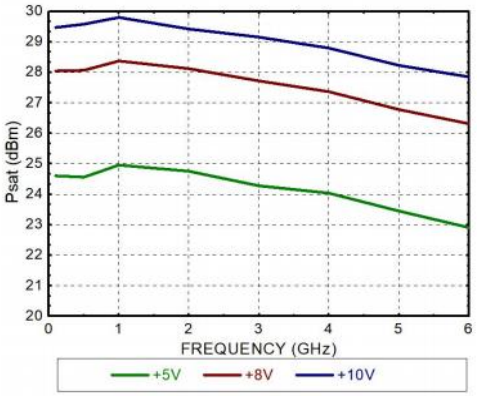
Return Loss&Reverse Isolation VDD=+10v



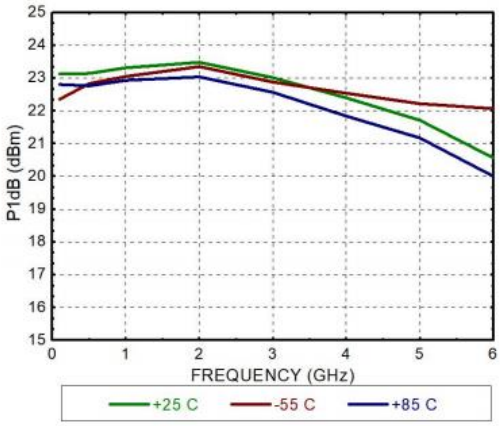
P1dB vs. VDD



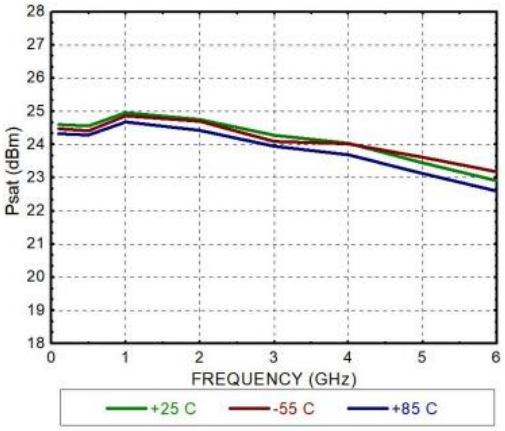
Psat vs. VDD



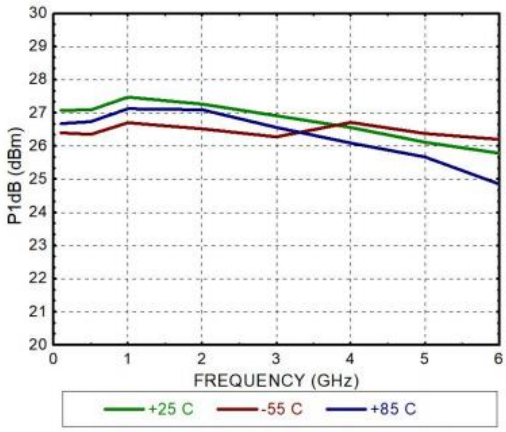
P1dB vs. Temperature VDD=+5v



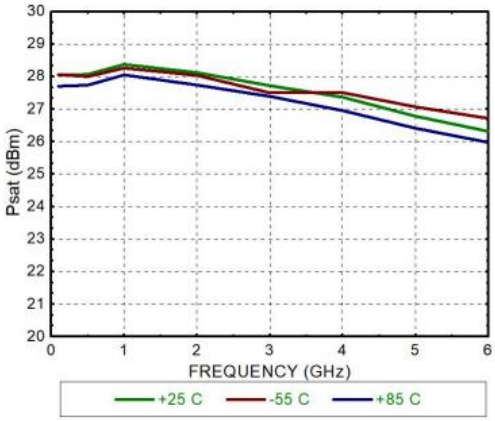
Psat vs. Temperature VDD=+5v



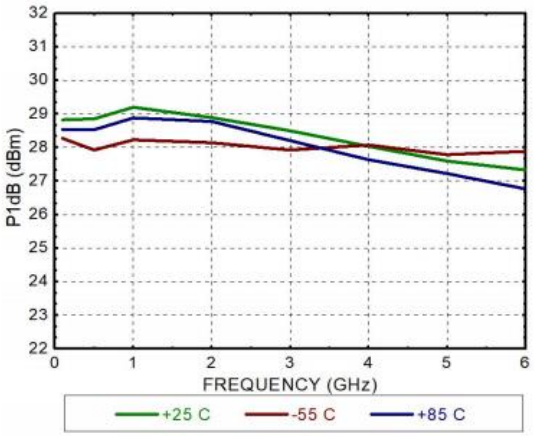
P1dB vs. Temperature VDD=+8v



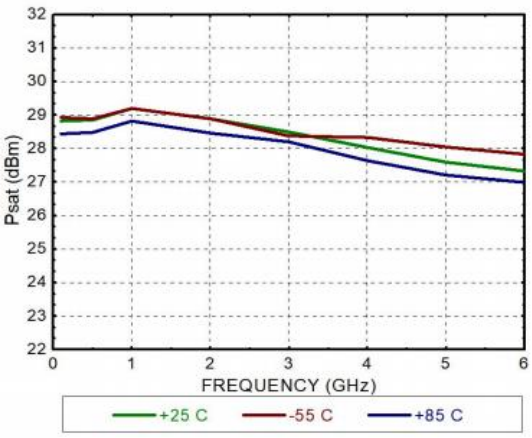
Psat vs. Temperature VDD=+8v



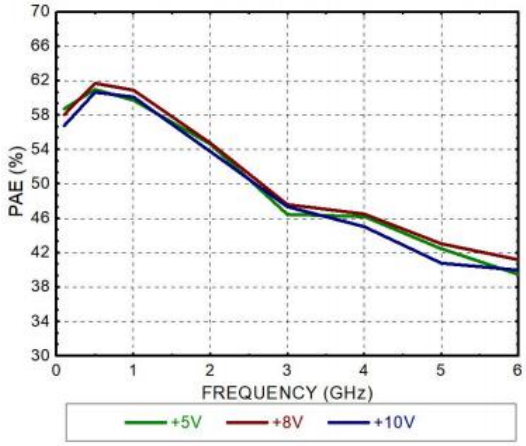
P1dB vs. Temperature VDD=+10v



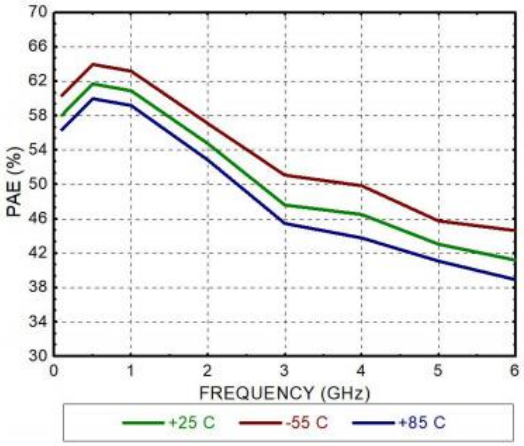
Psat vs. Temperature VDD=+10v



PAE @Psat vs. VDD

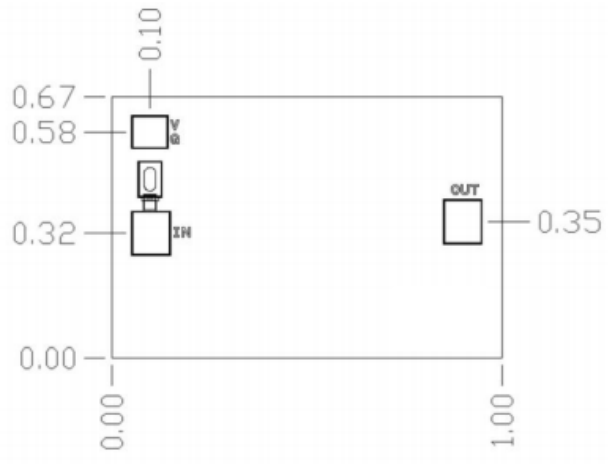


PAE @Psat vs. Tempersture VDD=+8V



Outline Drawing:

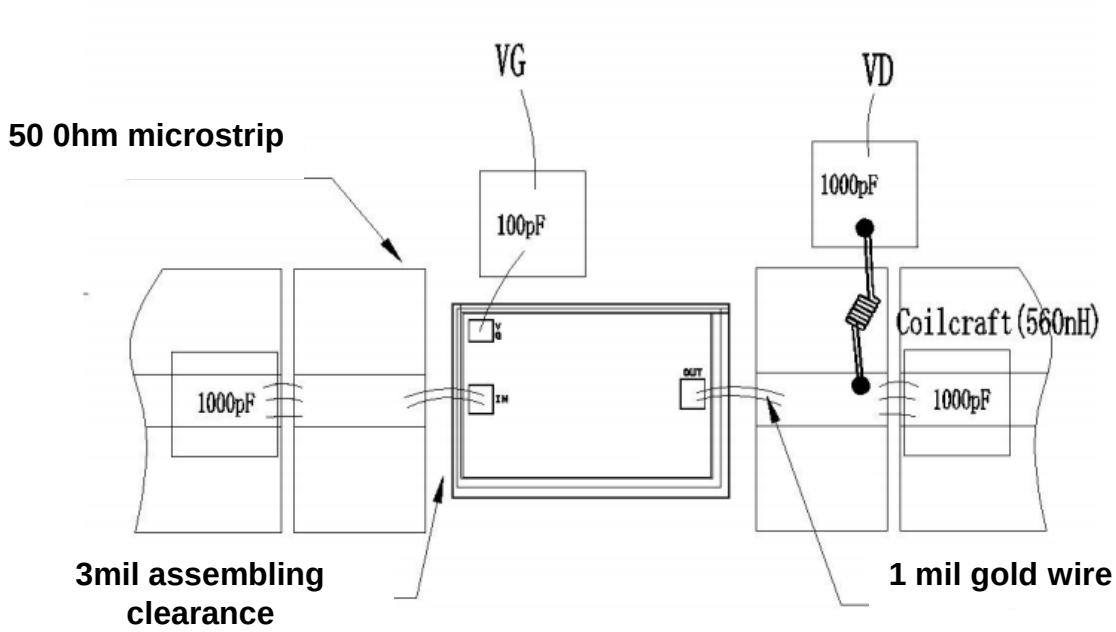
All Dimensions in um



Pad Description

PAD	Function	Description
1	IN	This pad is DC coupling, 50 ohm matched, blocking capacitors required
2	VG	This pad provides the amplifier gate control voltage, connected to external 100pF bypass capacitor.
3	OUT	This pad is DC coupling, 50 ohm matched, bias inductors and DC-blocking capacitors required
Die Bottom	GND	Die bottom must be connected to RF/DC ground

Assembly Drawing



Notes:

1. Die thickness: 100um
2. Typical bond pad is 100*100 μm²
3. Bond pad metalization: Gold
4. Backside metalization: Gold
5. Backside of the die (GND)
6. No connection required for unlabeled bond pads

Maximum Ratings:

1. Power supply voltage: +12V
2. RF input power: +20dBm
3. Operating temperature: -55℃ to +85℃
4. Storage temperature: -65℃ to +150℃