

GaAs QFN 3x3mm Driver Amplifier DC-6GHz

Features

• Frequency: DC-6GHz

Small Signal Gain: 21dB Typical
Gain Flatness: ±0.3dB Typical
Noise Figure:1.0dB Typical
P1dB: +28 dBm @VD=+10V

Psat: +29 dBm @VD=+10V

· Supply voltage:

VD = +5V/+8V/+10V@125mA VG = -0.8V to -0.2V

• Input/Output: 50Ω

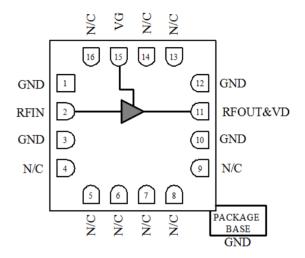
• Package Size: 3x3x0.7mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Electrical Specifications

Functional Block Diagram



TA = +25°C, VD= +5V/+8V/10V, VG=-0.8 to -0.2V, IDD = 125mA* Typical

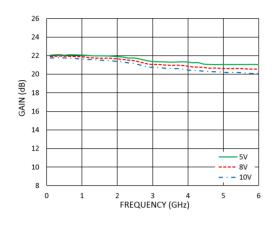
Parameters		VD=+5V			VD=+8V			VD=+10V		I I o i A o
		Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Frequency				ı	DC - (6				GHz
Small Signal Gain		21			21			21		dB
Gain Flatness		±0.3			±0.4			±0.4		dB
Noise Figure		1.0			1.0			1.0		dB
P1dB - Output 1dB Compression		22.5			26.5			28		dBm
Psat - Saturated Output Power		23.5			27.5			29		dBm
OIP3 - Output Third Order Intercept		35			39			40.5		dBm
Input Return Loss		15			15			15		dB
Output Return Loss		15			15			15		dB

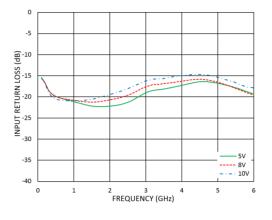
^{*}The operating current can be controlled around 125mA by adjusting the VG voltage, and the VG regulation range: -0.8V ~-0.2V.

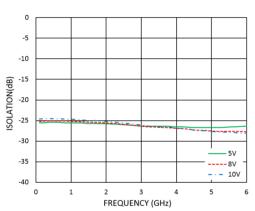


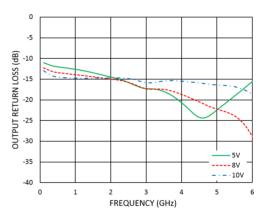
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Measurement Plots: S-parameters



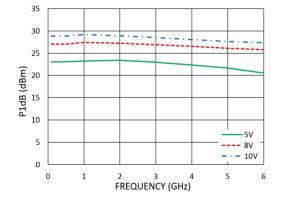


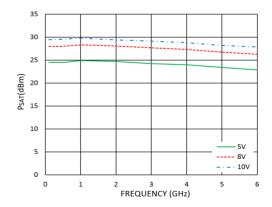




Measurement Plots: P1dB

Measurement Plots: PSAT



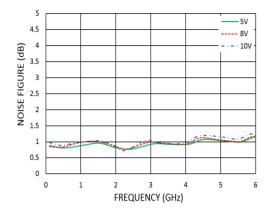


Sales: sales@millermmic.com



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Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+12V
Gate Bias Voltages(VG)	-3V
RF Input Power (RFIN)(VD=+10V)	+20 dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 16.7mW/°C above 85 °C)	1.5W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD

VG (V)	VD (V)	IDD (mA)		
-0.8 to -0.2	+5/+8/+10	125		



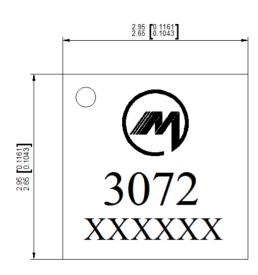
ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

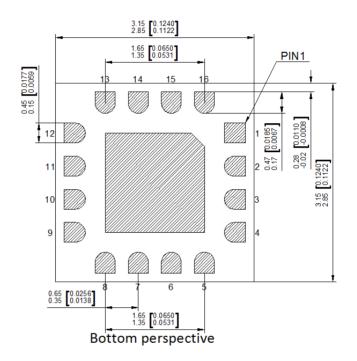


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Outline Drawing:

All Dimensions in mm[inches]





243 443	
90.	
212	
000	

Notes:

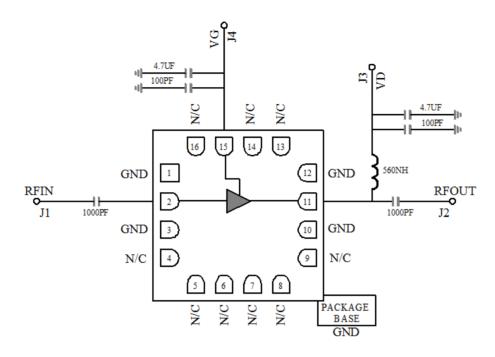
- 1. Package body material : Alumina.
- 2. Lead and ground paddle plating: Gold flash over nickel.
- 3. Dimensions are in millimeters(inches).
- 4. Lead spacing tolerance is non-cumulative.



V1 0

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Assembly Drawing



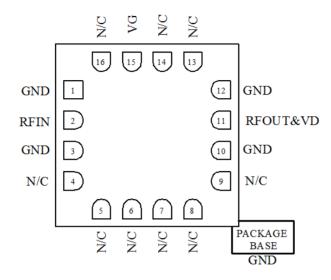
Pin Descriptions

No	Function	Description
4,5,6,7,8,9,13,14,16	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
2	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
11		Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
15	VG	Connect to external 100pf and 4.7uf bypass capacitors.
1,3,10,12	GND	These pins & exposed ground paddle must be connected to RF/DC ground
	GND	Package bottom must be connected to RF/DC ground



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Biasing and Operation

Turn ON procedure:

- 1. Connect GND to RF and dc ground.
- 2. Set all the gate bias voltages, VG to -3V.
- 3. Set the drain bias voltages VD to +5V/+8V/+10V.
- 4. Increase the gate bias voltages to achieve a quiescent supply current of 125 mA.
- 5. Apply RF signal.

Turn OFF procedure:

- 1. Turn off the RF signal.
- 2. Decrease the gate bias voltages, VG to -3V to achieve a $l_{DQ} = 0$ mA (approximately).
- 3. Decrease the drain bias voltages to 0 V.
- 4. Increase the all gate bias voltages to 0 V.

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