

V1.0.0

GaAs QFN 5x5mm Low Noise Amplifier 0.1-20GHz

### **Features**

• Frequency: 0.1 - 20GHz

Small Signal Gain: 16.5dB Typical
Gain Flatness: ±1.0dB Typical
Noise Figure: 2.5dB Typical
P1dB: 16dBm Typical
Power Supply: +8V/67mA

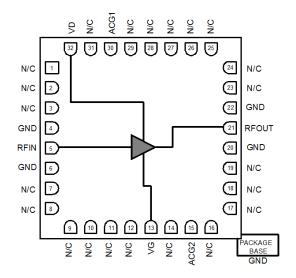
Input/Output: 50Ω

• Package Size: 5 x 5x 1mm

### **Typical Applications**

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

# **Functional Block Diagram**



## **Electrical Specifications**

TA = +25°C, VD = +8V, VG=-1V, IDD = 67mA Typical

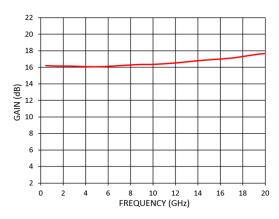
Parameters	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Frequency	0.1 - 6			6 - 12			12 - 20			GHz
Small Signal Gain	Small Signal Gain 15 16 15		15	16.5		15	17		dB	
Gain Flatness		±0.3			±0.5			±0.75		dB
Noise Figure		3			2			2.5		dB
P1dB - Output 1dB Compression	15	17.5		15	17		12	15		dBm
Past - Saturated Output Power		19			19			17		dBm
OIP3 - Output Third Order Intercept		26			26			24		dBm
Input Return Loss		18			18			18		dB
Output Return Loss		18			18			18		dB

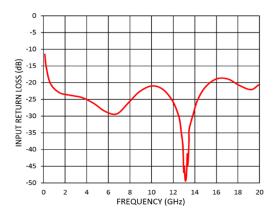
\* Adjust VG (-2V~-0V) to obtain device current of near 67mA.

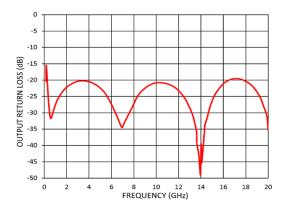
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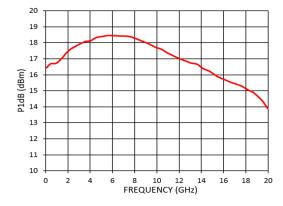
## **Measurement Plots: S-parameters**



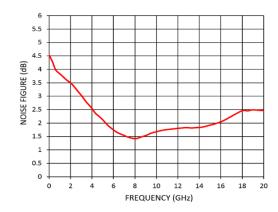




### **Measurement Plots: P1dB**



### **Measurement Plots: Noise Figure**



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### **Absolute Maximum Ratings**

Drain Bias Voltage (VD)	+9V
Gate Bias Voltages(VG)	–2V to 0 V
RF Input Power (RFIN)	+18dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 7mW/°C above 85 °C)	0.63W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150°C

# **Typical Supply Current vs. VD,VG**

VD (V)	VG (V)	IDD (mA)		
8	-1	67		



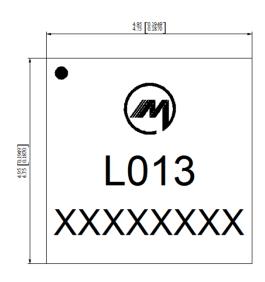
**ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS** 

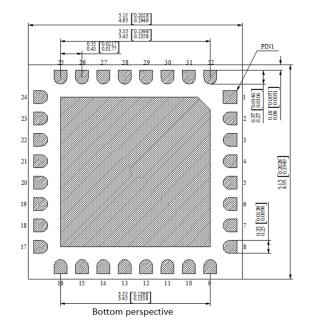
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# **Outline Drawing:**

All Dimensions in mm[inches]





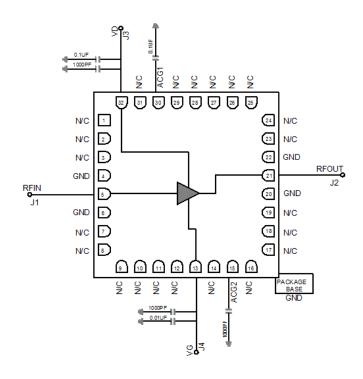
900	
22	
=8 I	

#### Notes:

- 1. Package body material: Alumina.
- 2. Lead and ground paddle plating: Gold flash over nickel.
- 3. Dimensions are in millimeters(inches).
- 4. Lead spacing tolerance is non-cumulative.



# **Assembly Drawing**

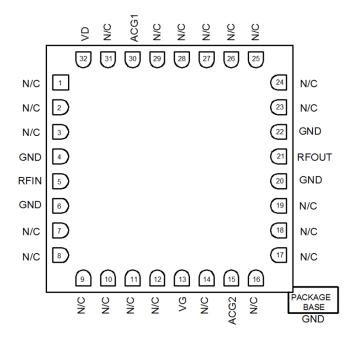


# **Pin Descriptions**

No	Function	Description
1,2,3,7,8,9,10,11,12,14,16 ,17,18,19,23,24,25,26,27, 28,29,31	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
5	RF IN	RF Signal Input. This pad is dc-coupled and matched to 50 $\Omega$ .
21	RF OUT	RF Signal Output. This pad is dc-coupled and matched to 50 $\Omega$ .
32	VD	Connect to external 1000pF and 0.1uF bypass capacitors.
13	VG	Connect to external 1000pF and 0.01uF bypass capacitors.
30	ACG1	Connect to external 0.1uF bypass capacitors.
15	ACG2	Connect to external 1000pF bypass capacitors.
4,6,20,22	GND	These pins & exposed ground paddle must be connected to RF/DC ground
	GND	Package bottom must be connected to RF/DC ground

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# **Biasing and Operation**

### Turn ON procedure:

- 1. Connect GND to RF and dc ground.
- 2. Set the gate bias voltage, VG to -2.0V.
- 3. Set the drain bias voltage, VD to +8V.
- 4. Increase the gate bias voltage to achieve a quiescent supply current of 67 mA.
- 5. Apply RF signal.

### Turn OFF procedure:

- 1. Turn off the RF signal.
- 2. Decrease the gate bias voltage, VG to -2.0V to achieve a  $\log = 0$  mA (approximately).
- 3. Decrease all of the drain bias voltage to 0 V.
- 4. Increase the gate bias voltage to 0 V.

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