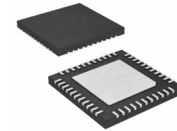
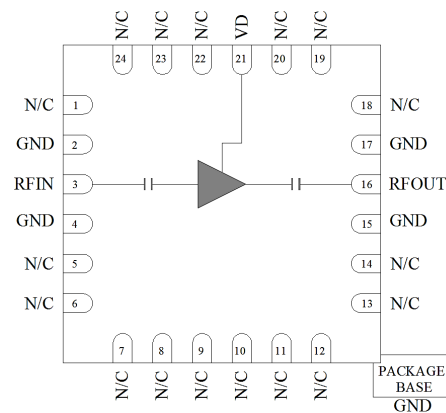


**Features**

- Single Biasing Voltage (Self Biased)
- Frequency: 1-9GHz
- Small Signal Gain: 28dB Typical
- Gain Flatness:  $\pm 0.75$ dB Typical
- Noise Figure: 0.7dB Typical
- P1dB: 17dBm Typical
- Power Supply: +5V/50mA
- Input/Output: 50 $\Omega$
- Package Size : 4 x 4 x 0.65mm


**Functional Block Diagram**

**Typical Applications**

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

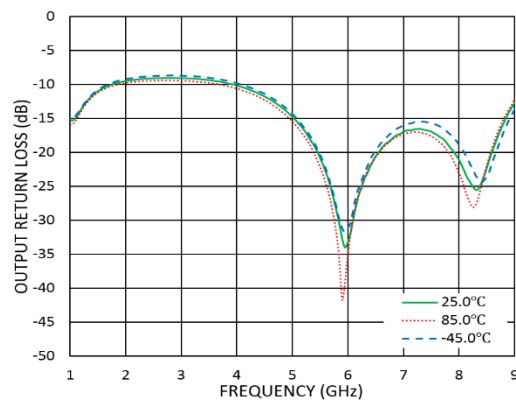
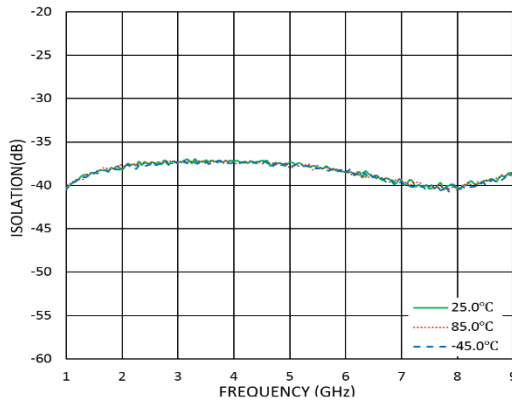
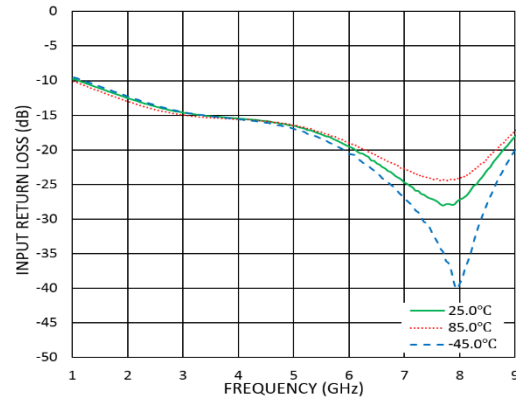
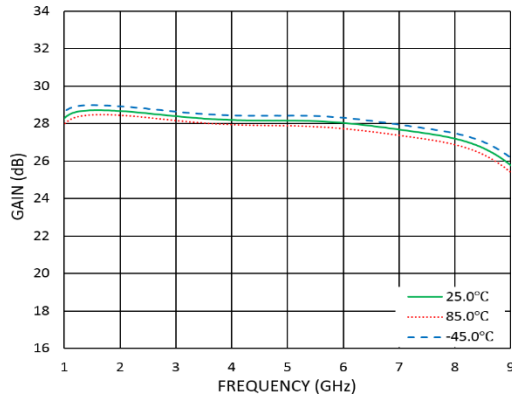
**Electrical Specifications**

TA = +25°C, VD = +5V, IDD = 50mA Typical

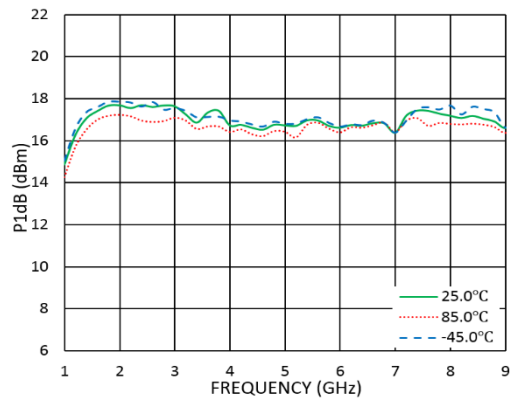
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	1		2	2		6	6		9	GHz
Small Signal Gain	27.5	28.5		27.0	28.0		24.5	27.0		dB
Gain Flatness		$\pm 0.5$			$\pm 0.5$			$\pm 1.0$		dB
Noise Figure		0.75	1.0		0.7	0.8		0.8	1.0	dB
P1dB - Output 1dB Compression	14.0	17.0		16.0	17.0		16.0	17.0		dBm
Psat - Saturated Output Power		18.5			18.0			18.5		dBm
OIP3 - Output 3rd Order Intercept		30.0			29.0			29.0		dBm
Input Return Loss		12.0			15.0			22.0		dB
Output Return Loss		10.0			10.0			20.0		dB



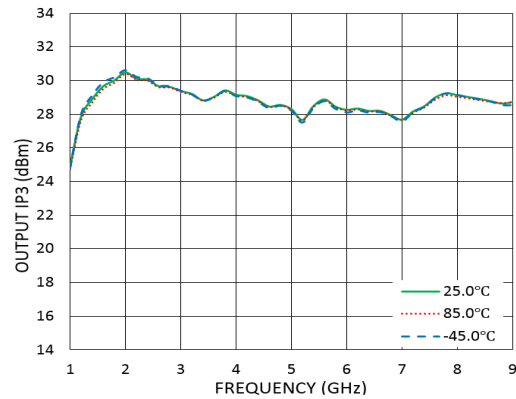
### Measurement Plots: S-parameters

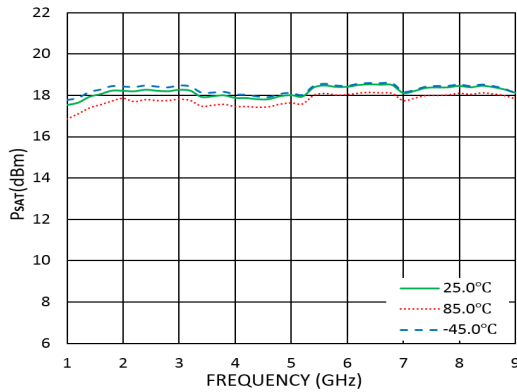
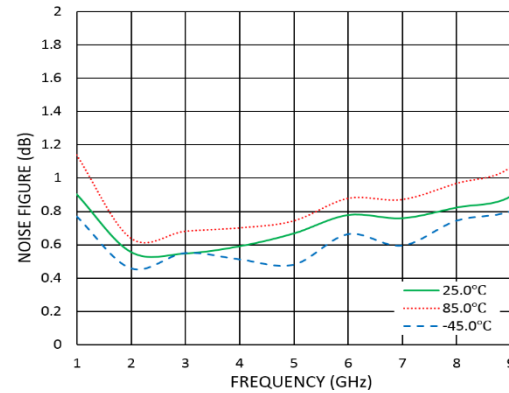


### Measurement Plots: P1dB



### Measurement Plots: OIP3



**Measurement Plots: Psat**

**Measurement Plots: Noise Figure**

**Absolute Maximum Ratings**

Drain Bias Voltage (VD)	+7V
RF Input Power (RFIN)(VD=+5V)	+20dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 4.4mW/°C above 85 °C)	0.4W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

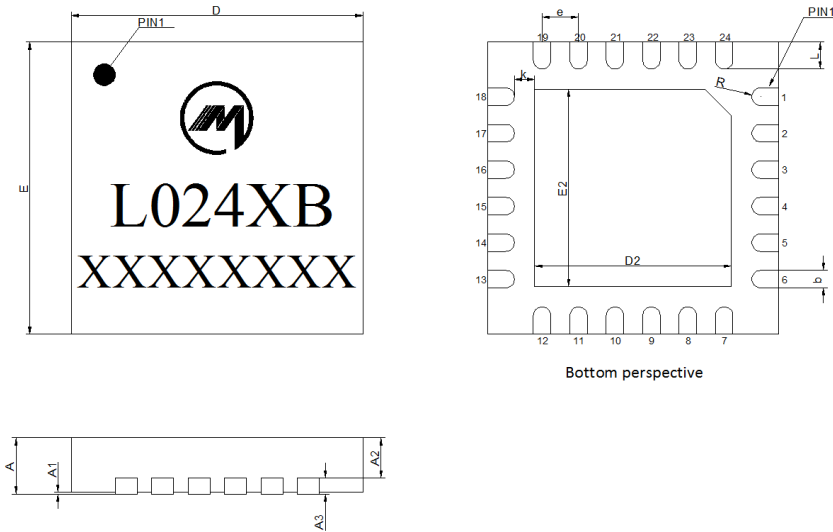
**Typical Supply Current vs. VD**

VD (V)	IDD (mA)
+5	50


ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS



**Outline Drawing:**  
All Dimensions in mm



UNITS=MM

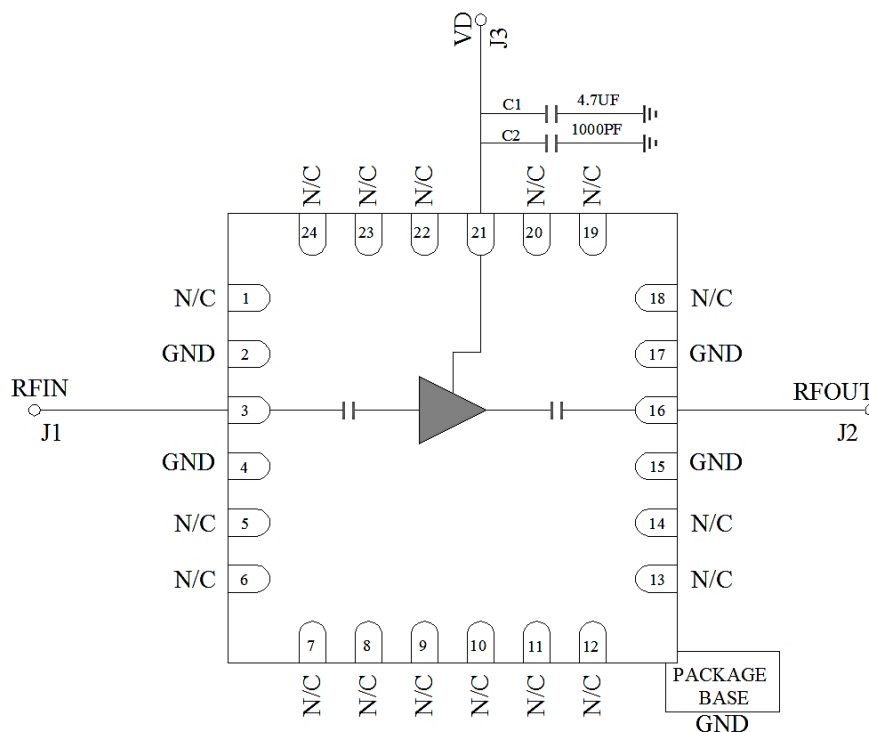
SYMBOL	MIN	NOM	MAX
A	0.55	0.65	0.75
A1	0	0.02	0.05
A2	0.36	0.45	0.54
A3	0.19	0.20	0.21
D	3.90	4.00	4.10
E	3.90	4.00	4.10
b	0.19	0.24	0.29
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50	
K	0.20		
L	0.35	0.40	0.45
R	0.10		

**Notes:**

1. Package model : 24-Lead Lead Frame Chip Scale Package .
2. Dimensions are in millimeters.
3. Lead spacing tolerance is non-cumulative.

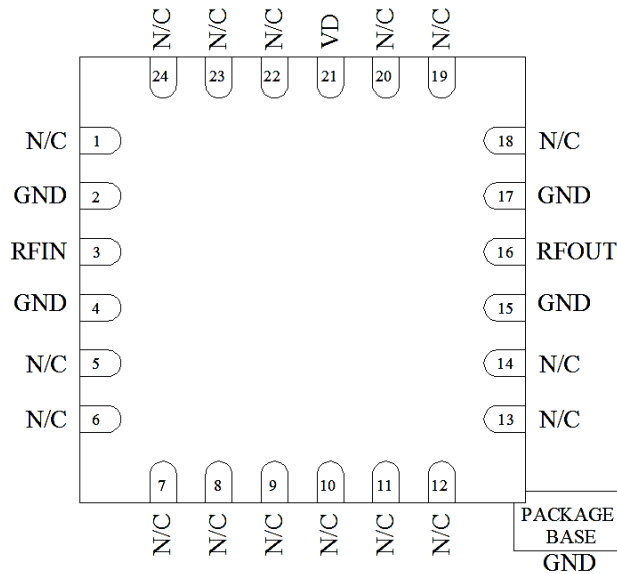


### Assembly Drawing



### Pin Description

No	Function	Description
1,5,6,7,8,9,10,11,12,13,14,18,19,20,22,23,24	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
3	RF IN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
16	RF OUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
21	VD	Connect to external 1000pf and 4.7uf bypass capacitors.
2,4,15,17	GND	These pins & exposed ground paddle must be connected to RF/DC ground
25	GND	Package bottom must be connected to RF/DC ground



## Biasing and Operation

### Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Apply positive drain voltage  $V_D$  and set to +5.0 V .
3. Apply RF signal.

### Turn OFF procedure:

1. Turn off the RF signal.
2. Turn off the positive drain voltage  $V_D$ .

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