

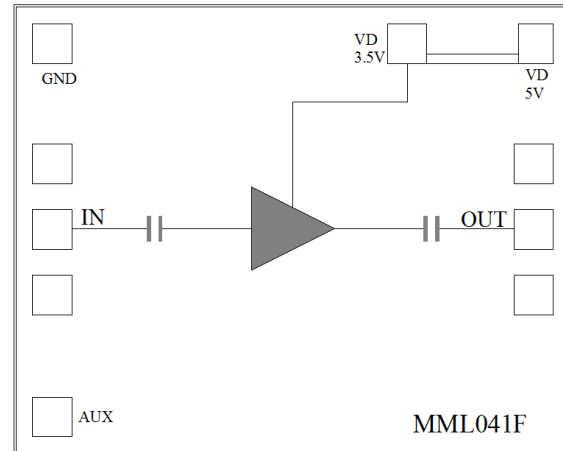
Features

- Single Biasing Voltage (Self Biased)
- Frequency: 5-20GHz
- Small Signal Gain Typical :
25dB@6GHz
21dB@18GHz
- Gain Flatness: ± 2.0 dB Typical
- Noise Figure: 1.5dB Typical
- P1dB: 16dBm Typical
- Power Supply: +3.5V@77mA;+5V@80mA
- Input/Output: 50 Ω
- Chip Size: 1.28 x 1.03 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram



Electrical Specifications

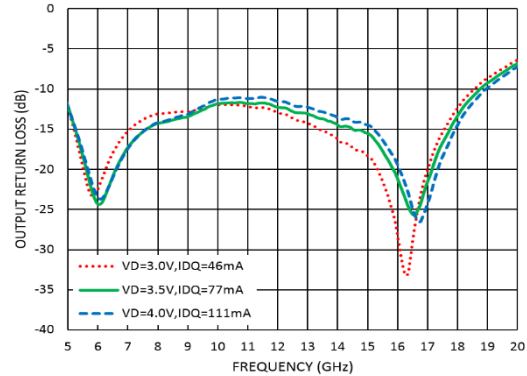
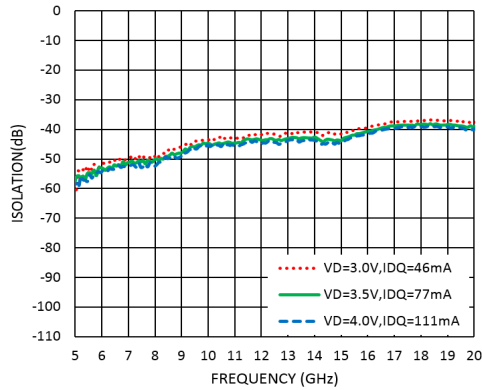
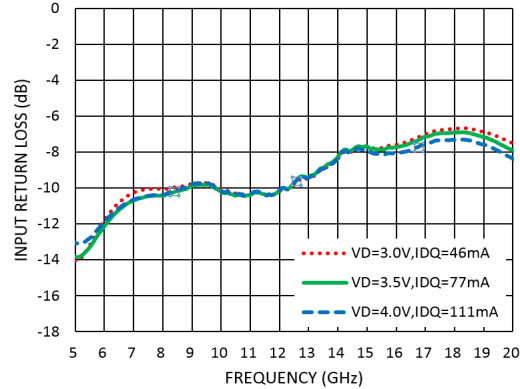
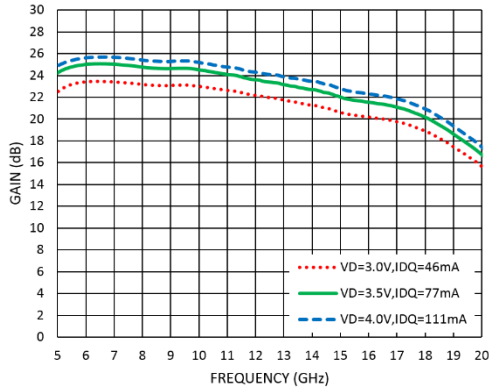
TA = +25°C, VD = +3.5V/+5V, IDD = 77/80mA Typical

Parameters	VD=3.5V						VD=5V						Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency	5-12			12-20			5-12			12-20			GHz
Small Signal Gain	23	24		16	20		23	24		16.5	21		dB
Gain Flatness		± 1.0			± 3.0			± 1.0			± 3.0		dB
Noise Figure		1.6	2.3		1.8	2.8		1.6	2.5		1.8	2.5	dB
P1dB-Output 1dB Compression	13.5	15		15	16.5		13.5	15.5		12.5	16		dBm
Psat - Saturated Output Power		16.5			17.5			17			18		dBm
OIP3- Output Third Order Intercept		25.5			29			26.5			30		dBm
Input Return Loss		-10			-7			-9			-7		dB
Output Return Loss		-12			-12			-15			-10		dB



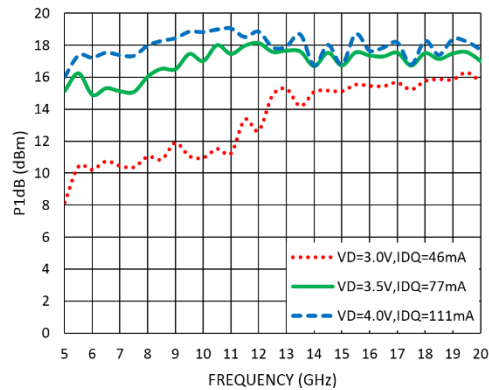
Measurement Plots: S-parameters

VD=3.5V



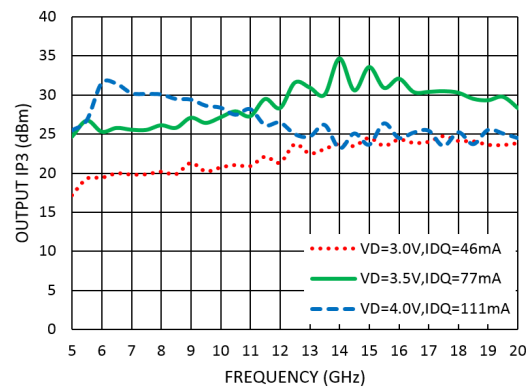
Measurement Plots: P1dB

VD=3.5V

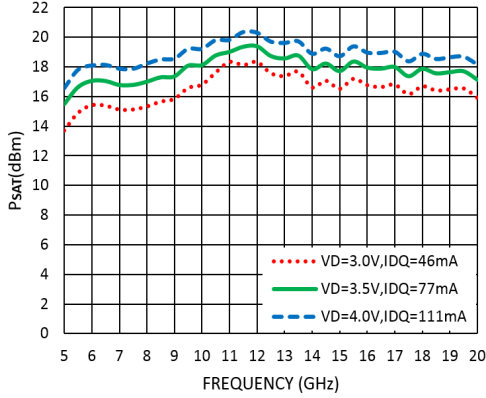


Measurement Plots: OIP3

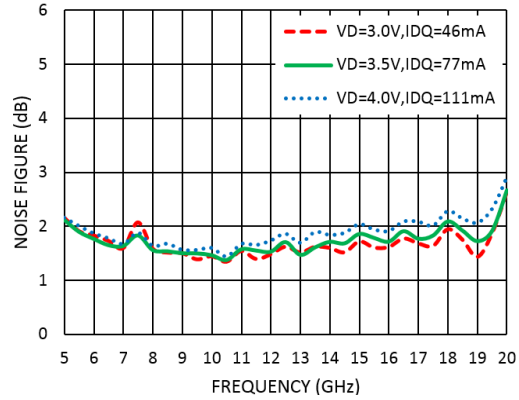
VD=3.5V



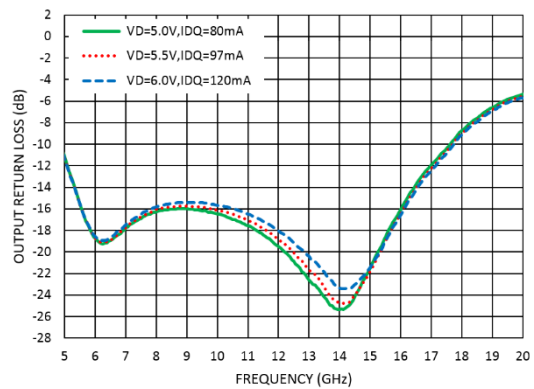
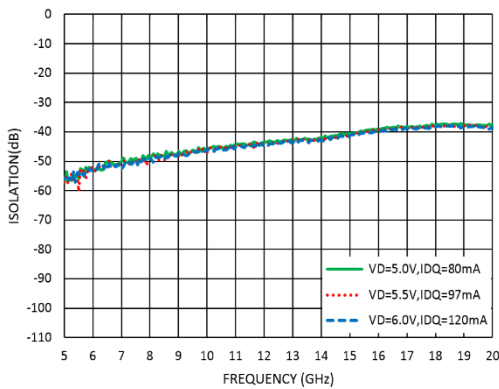
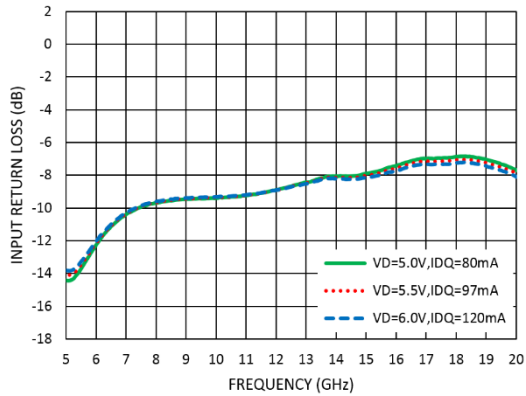
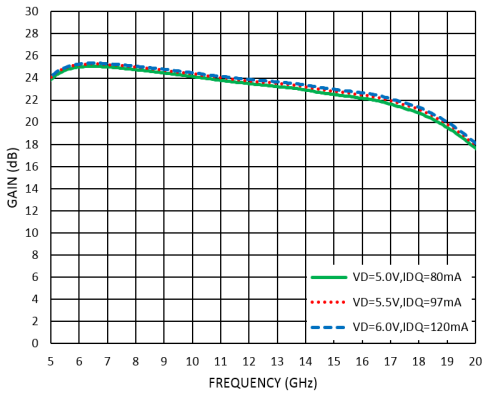
Measurement Plots: PSAT
VD=3.5V

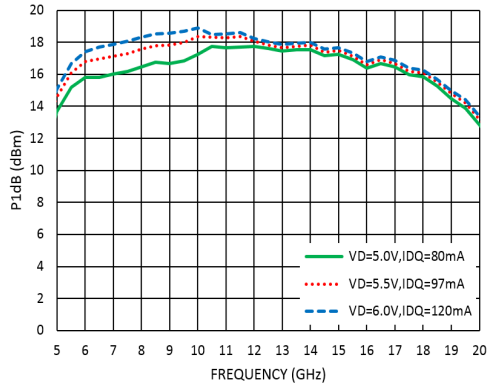
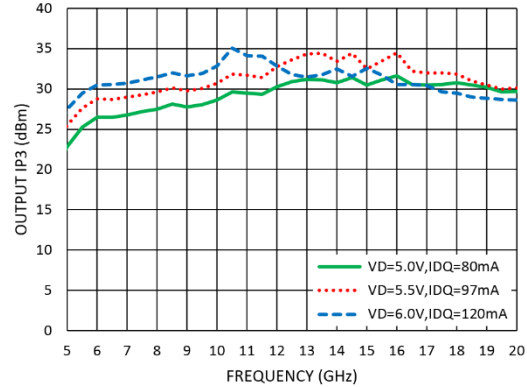
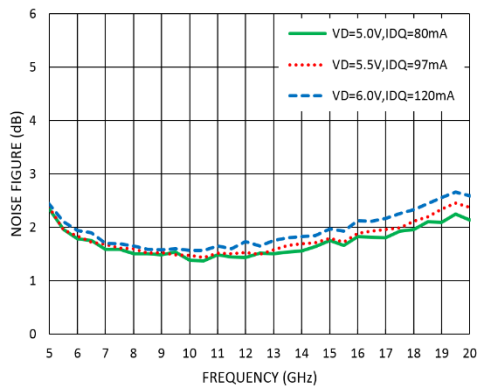


Measurement Plots: Noise Figure
VD=3.5V



Measurement Plots: S-parameters
VD=5V



**Measurement Plots: P1dB
VD=5V**

**Measurement Plots: OIP3
VD=5V**

**Measurement Plots: Noise Figure
VD=5V**

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+3.5V	+6V
	+5V	+7V
RF Input Power (RFIN)(VD)	+20dBm	
Channel Temperature	150 °C	
Continuous P _{diss} (T = 85 °C)(derate 11.7 mW/°C above 85 °C)	1.05W	
Thermal Resistance (channel to die bottom)	50°C/W	
Operating Temperature	-55 to +85 °C	
Storage Temperature	-65 to +150 °C	

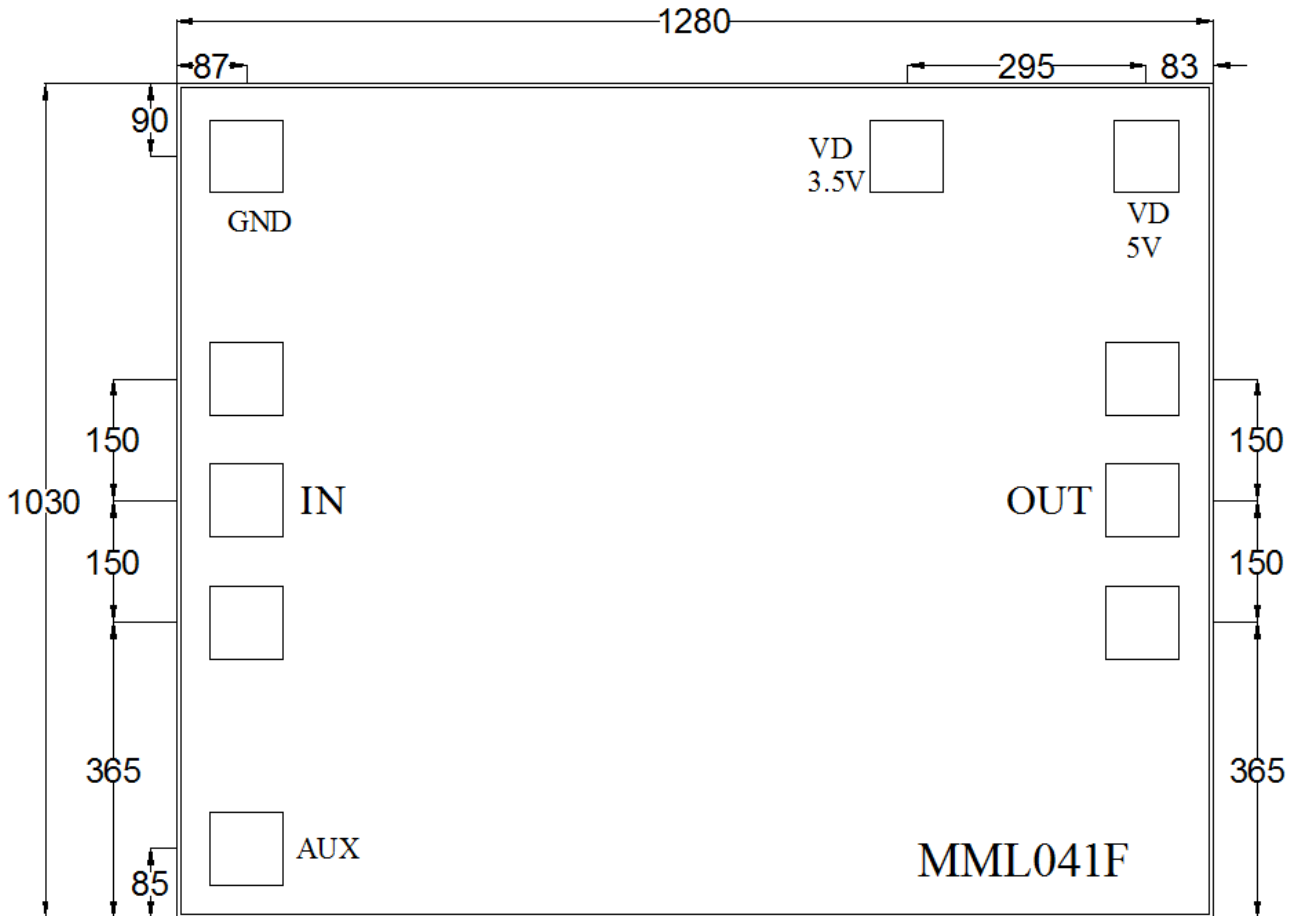
Typical Supply Current vs. VD

VD (V)	IDD (mA)
+3.0	46
+3.5	77
+4.0	111
+5.0	80
+5.5	97
+6.0	120


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing:
All Dimensions in μm

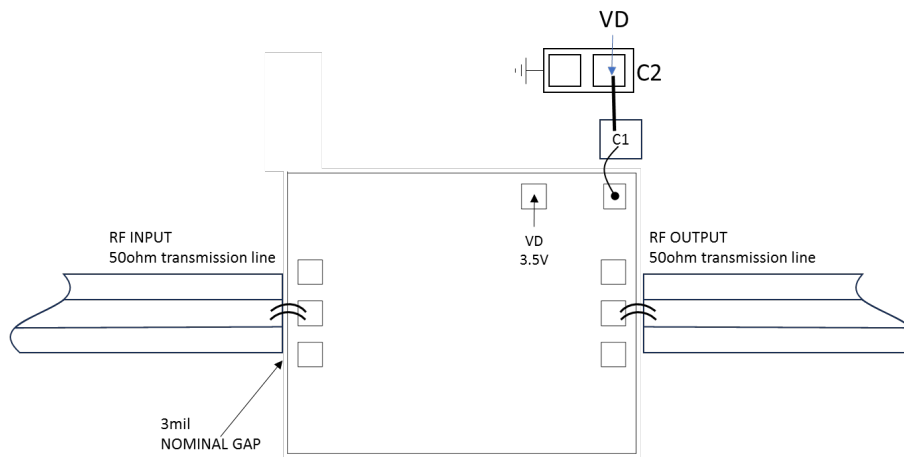
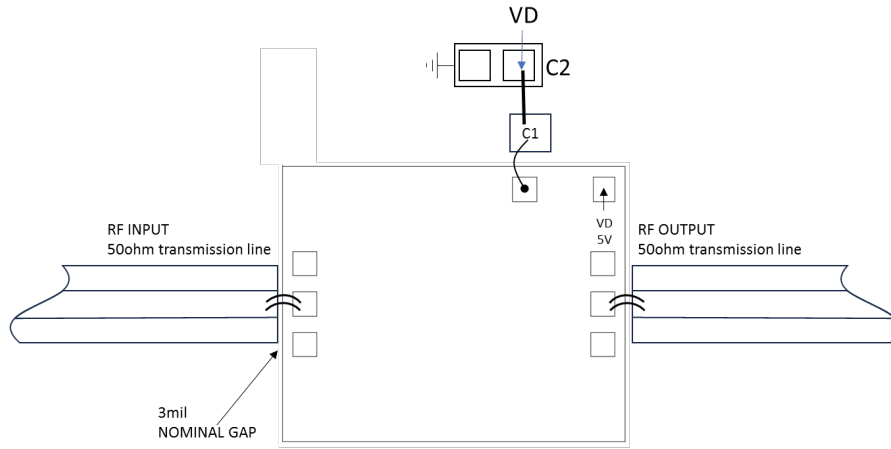


Notes:

1. Die thickness: 100 μm
2. VD bond pad is 90*90 μm^2
3. RF IN/OUT bond pad is 90*90 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold

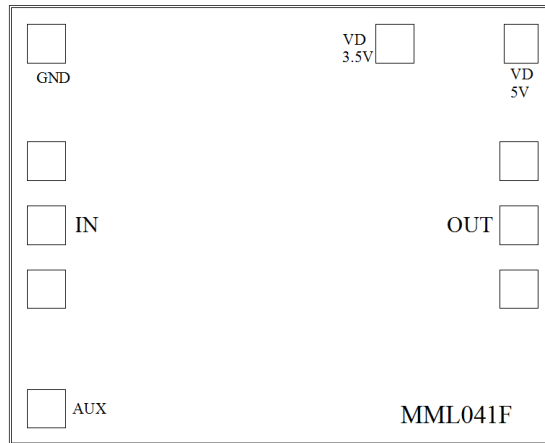


Assembly Drawing



Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1
C2	0.1 μ F Example: Murata Electronics Part: GRM033Z71C104KE14D (0201)

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Connect to external 100pF and 0.01uF bypass capacitors
4	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect Input and Output with 50 Ohm source/load.
2. Apply positive drain voltage to +3.5V(VD) or +5.0 V (VD)
3. Apply RF signal.

Turn OFF procedure:

1. Turn off RF signal
2. Turn off positive drain voltage VD

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