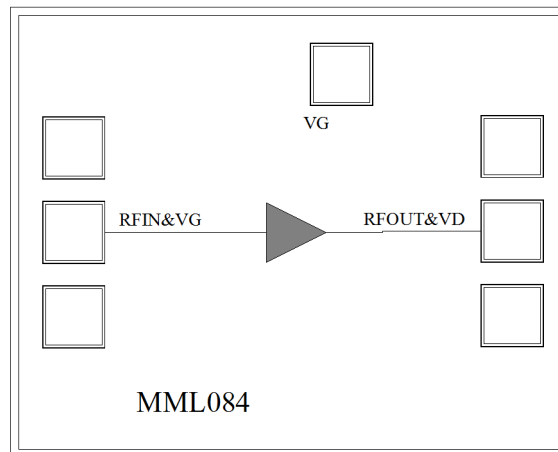


Features

- Frequency: 0.1-18GHz
- Small Signal Gain: 15.5dB Typical
- Gain Flatness: ± 1.0 dB Typical
- Noise Figure: 1.5dB Typical
- P1dB: 17dBm Typical
- Power Supply:
VD=+5V@37mA ,VG=+0.5V
- Input/Output: 50 Ω
- Chip Size: 0.995 x 0.8 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

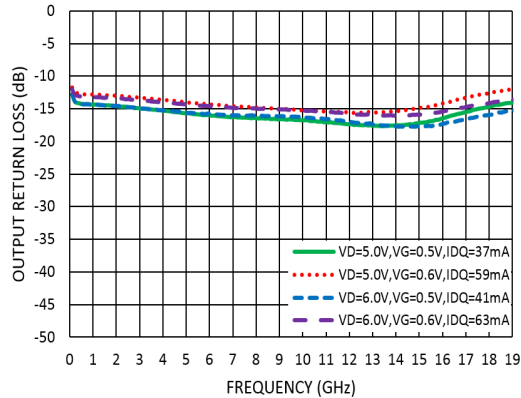
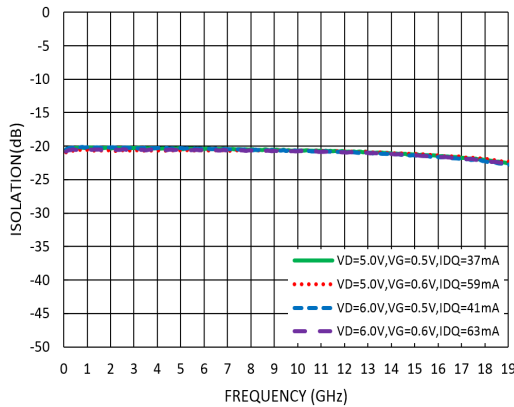
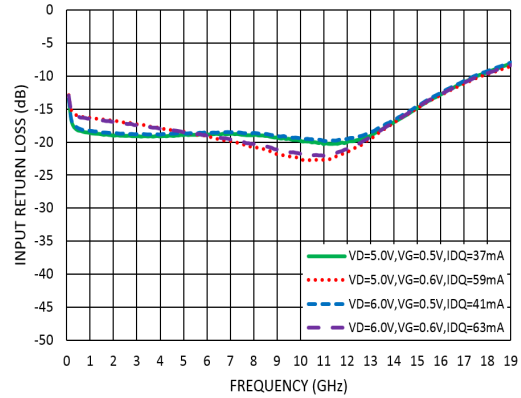
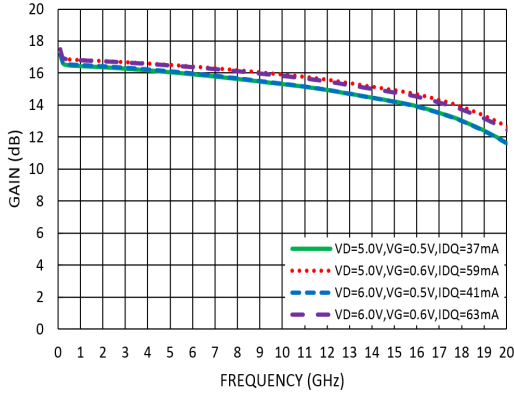
Functional Block Diagram

Electrical Specifications

TA = +25°C, VD = +5V , VG=+0.5V , IDD = 37mA Typical

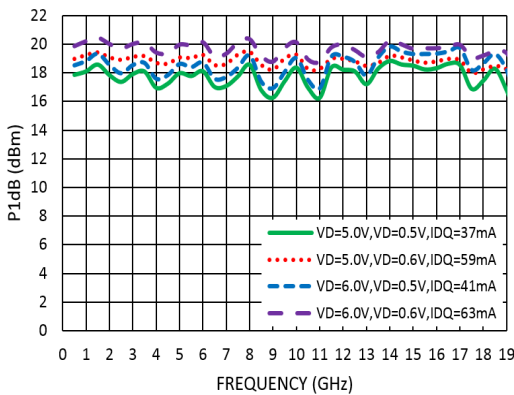
Parameters	Min.	Typ.	Max.	Units
Frequency	0.1		18	GHz
Small Signal Gain	13	15.5		dB
Gain Flatness		± 1.0		dB
Noise Figure		1.5	2.0	dB
P1dB - Output 1dB Compression	15	17		dBm
Psat - Saturated Output Power		19		dBm
OIP3 - Output Third Order Intercept		28		dBm
Input Return Loss		-17		dB
Output Return Loss		-15		dB



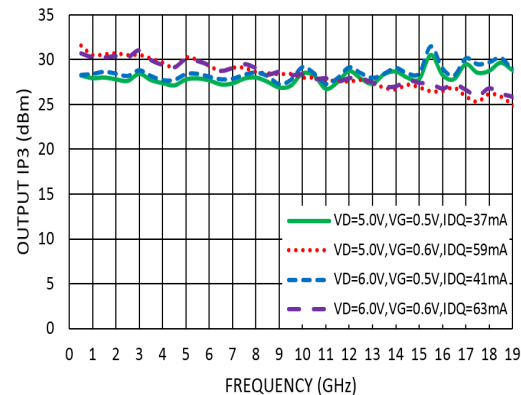
Measurement Plots: S-parameters

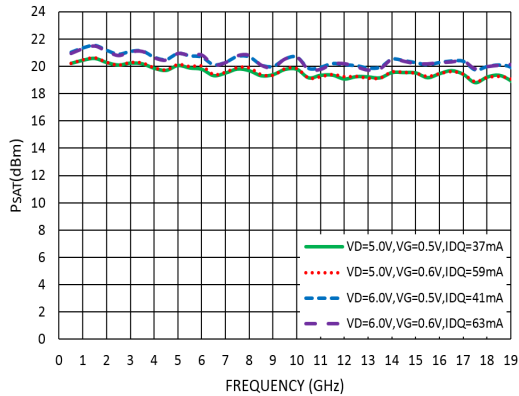
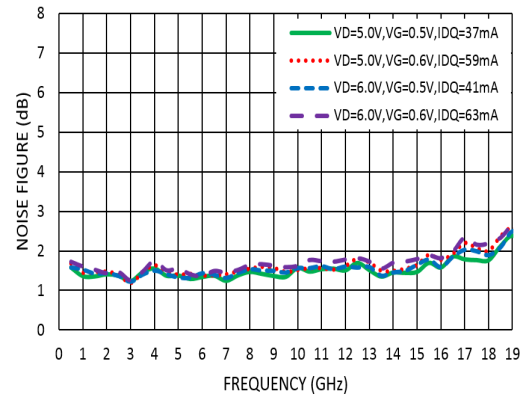


Measurement Plots: P1dB



Measurement Plots: OIP3



Measurement Plots: PSAT

Measurement Plots: Noise Figure

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+7V
Gate Bias Voltage (VG)	+1V
RF Input Power (RFIN)	+20dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 5.5mW/°C above 85 °C)	0.5W
Thermal Resistance (channel to die bottom)	60°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

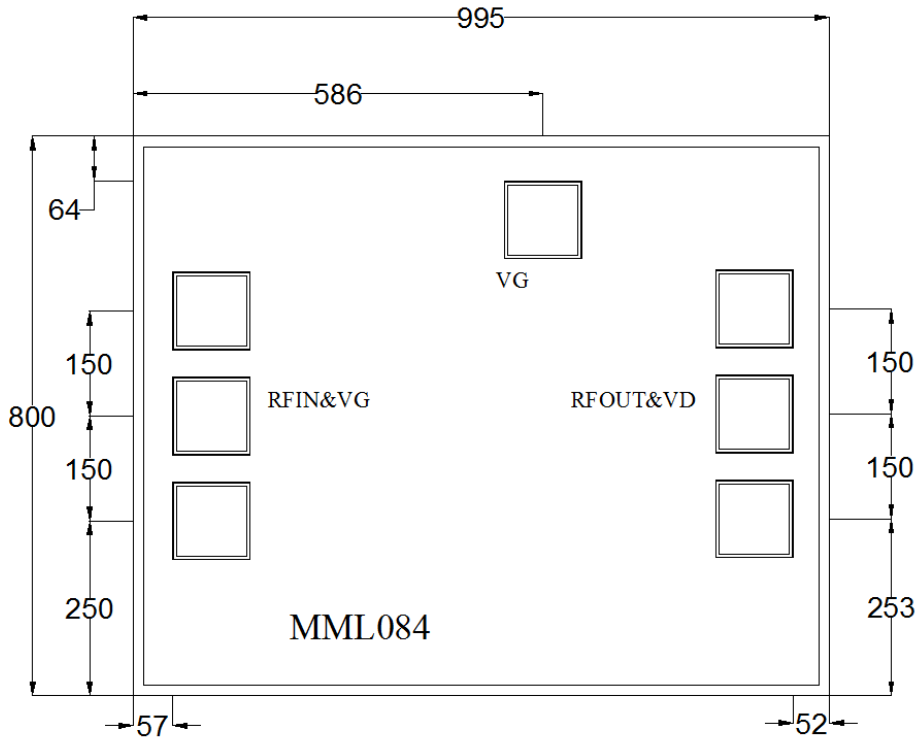
Typical Supply Current vs. VD, VG

VD (V)	VG (V)	IDD (mA)
+5	+0.5	37
+5	+0.6	59
+6	+0.5	41
+6	+0.6	63


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing:
All Dimensions in μm

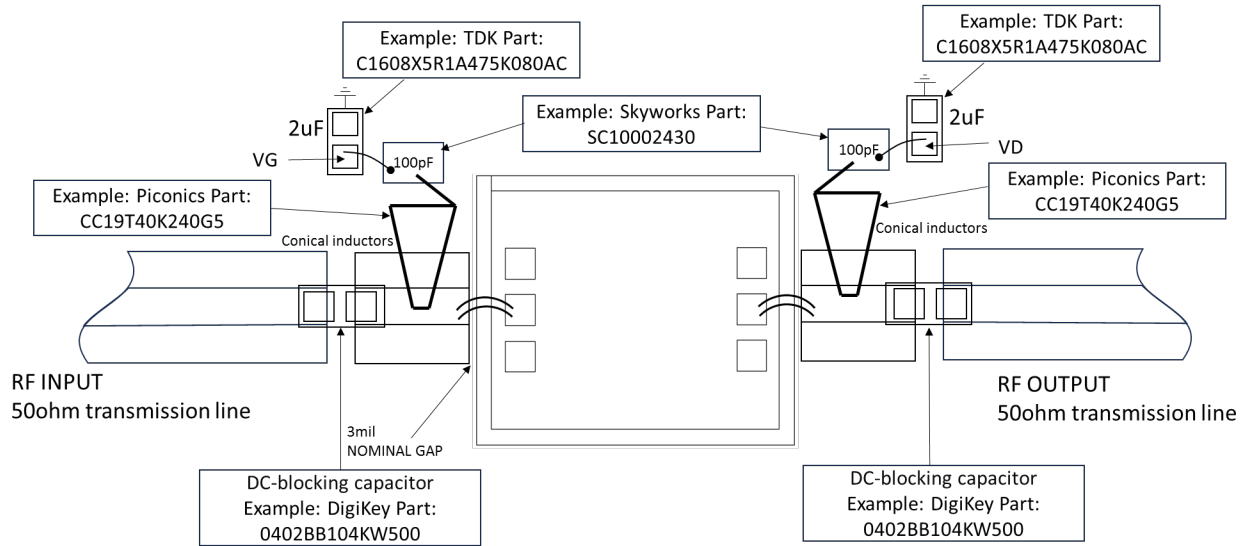


Notes:

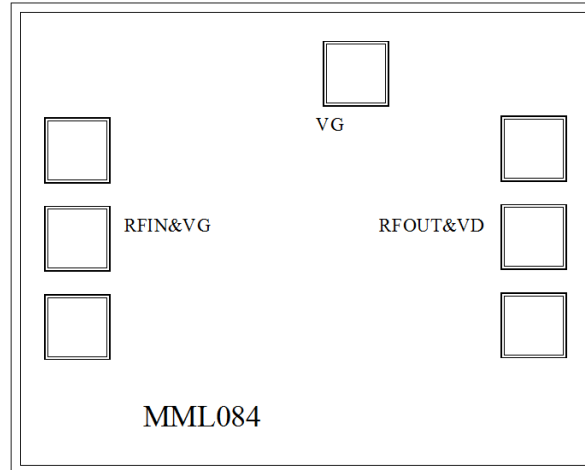
1. Die thickness: 100 μm
2. DC bond pad is 100*100 μm^2
3. RF IN/OUT bond pad is 100*100 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold



Assembly Drawing



No	Function	Description
1	RF IN & VG	RF signal input terminal; connected to 50Ω circuit; blocking capacitor required; The gate bias of the amplifier requires an external inductor and 100pF, 2uF bypass capacitors.
2	RF OUT & VD	RF signal output terminal; connected to 50Ω circuit; blocking capacitor required; The amplifier drain bias requires an external inductor and 100pF, 2uF bypass capacitors.
3	VG	N/A
4	Die Bottom	Die bottom must be connected to RF and dc ground.



Biassing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VG to +0V.
3. Set the drain bias voltages VD to +5V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 37 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to +0V to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.

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