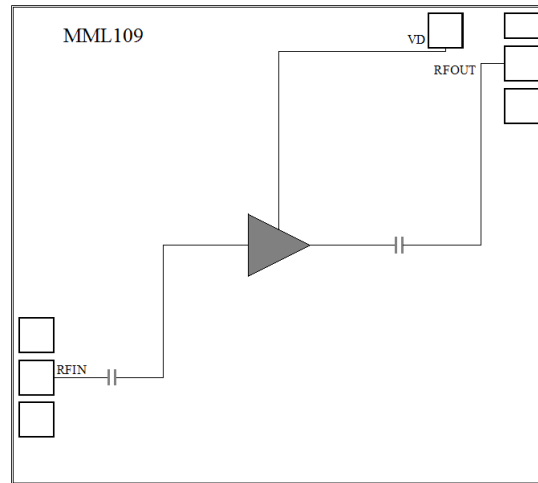


Features

- Single Biasing Voltage (Self Biased)
- Frequency: 5-50GHz
- Small Signal Gain: 11.5dB Typical
- Gain Flatness: ± 0.5 dB Typical
- Noise Figure: 2.5dB Typical
- P1dB: 12dBm Typical
- Power Supply: +5V@50mA
- Input/Output: 50 Ω
- Chip Size: 1.52 x 1.36 x 0.1mm

Typical Applications

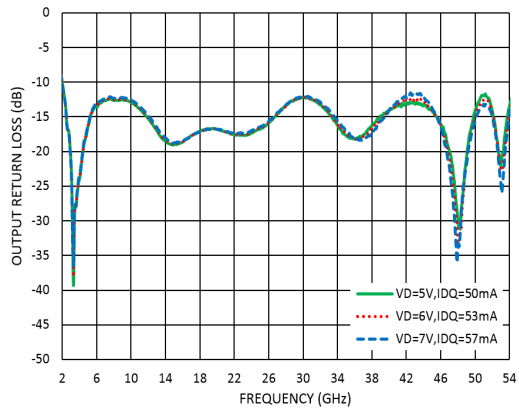
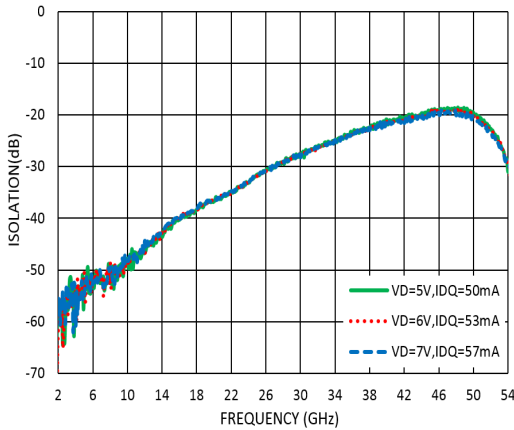
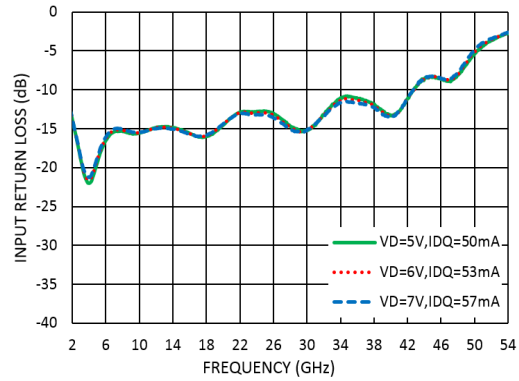
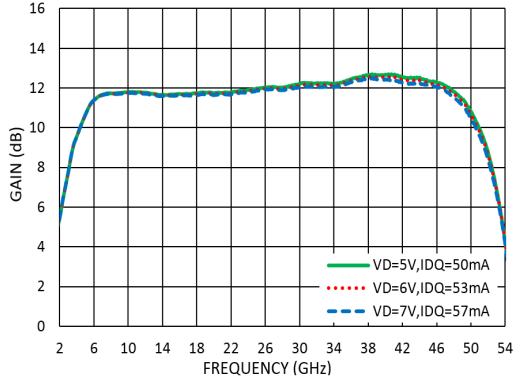
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

Electrical Specifications
TA = +25°C, VD = +5V, IDD = 50mA Typical

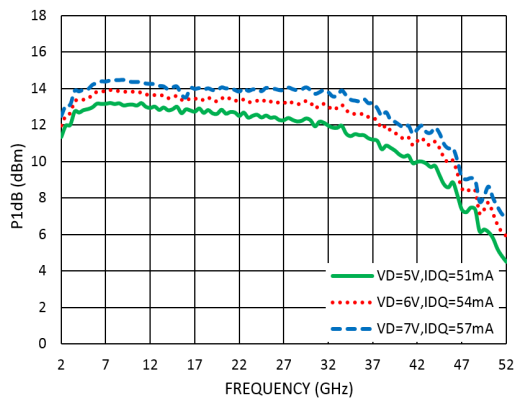
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	5		30	30		50	GHz
Small Signal Gain	10	11.5		10	12		dB
Gain Flatness		± 0.5			± 0.5		dB
Noise Figure		2.5			5.5		dB
P1dB - Output 1dB Compression	11	12		5	9		dBm
Psat - Saturated Output Power		15			13		dBm
OIP3 - Output Third Order Intercept		23			23		dBm
Input Return Loss		-14			-10		dB
Output Return Loss		-13			-12		dB



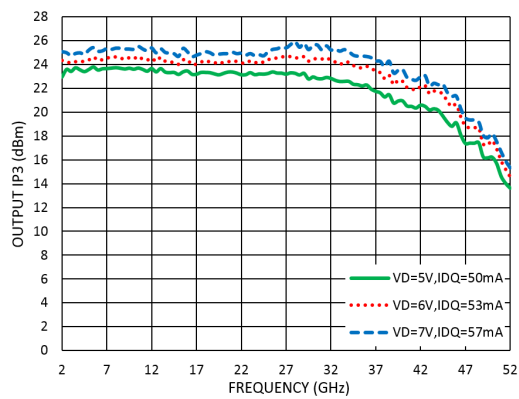
Measurement Plots: S-parameters



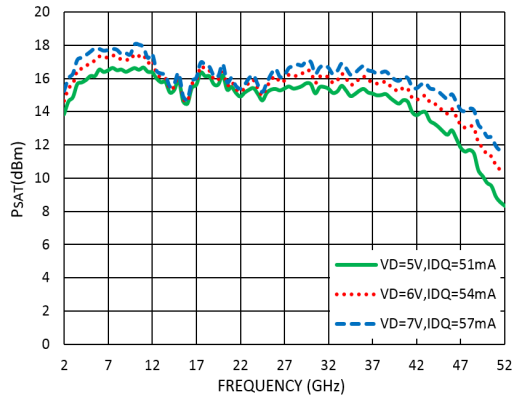
Measurement Plots: P1dB



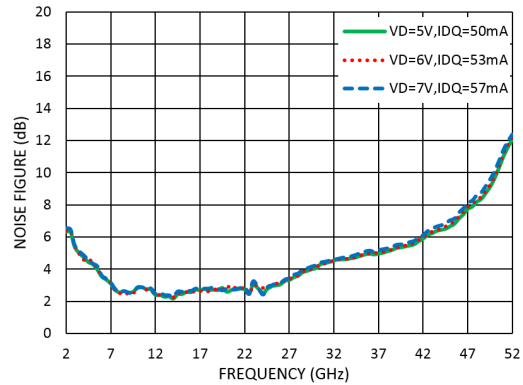
Measurement Plots: OIP3



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+9V
RF Input Power (RFIN)	+23dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 4.3mW/°C above 85 °C)	0.59W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +125 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD

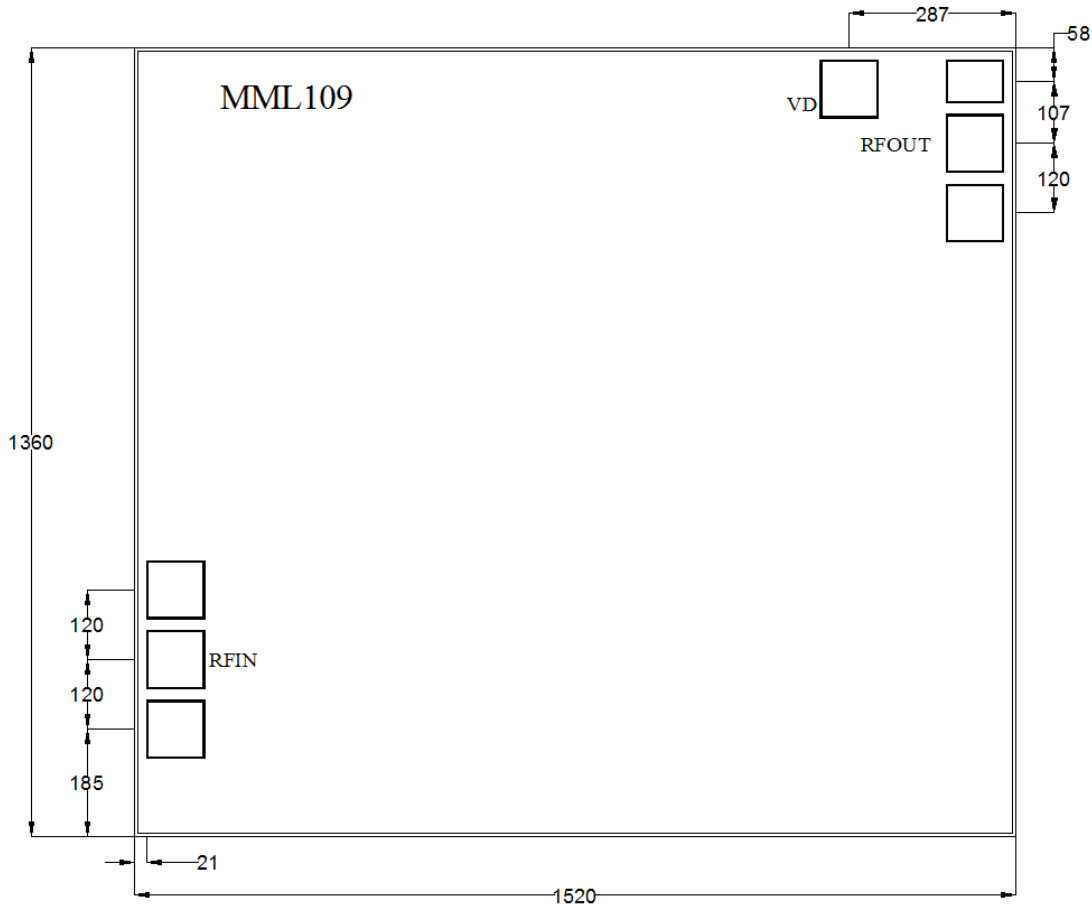
VD (V)	IDD (mA)
+5	50
+6	53
+7	57



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing:
All Dimensions in μm

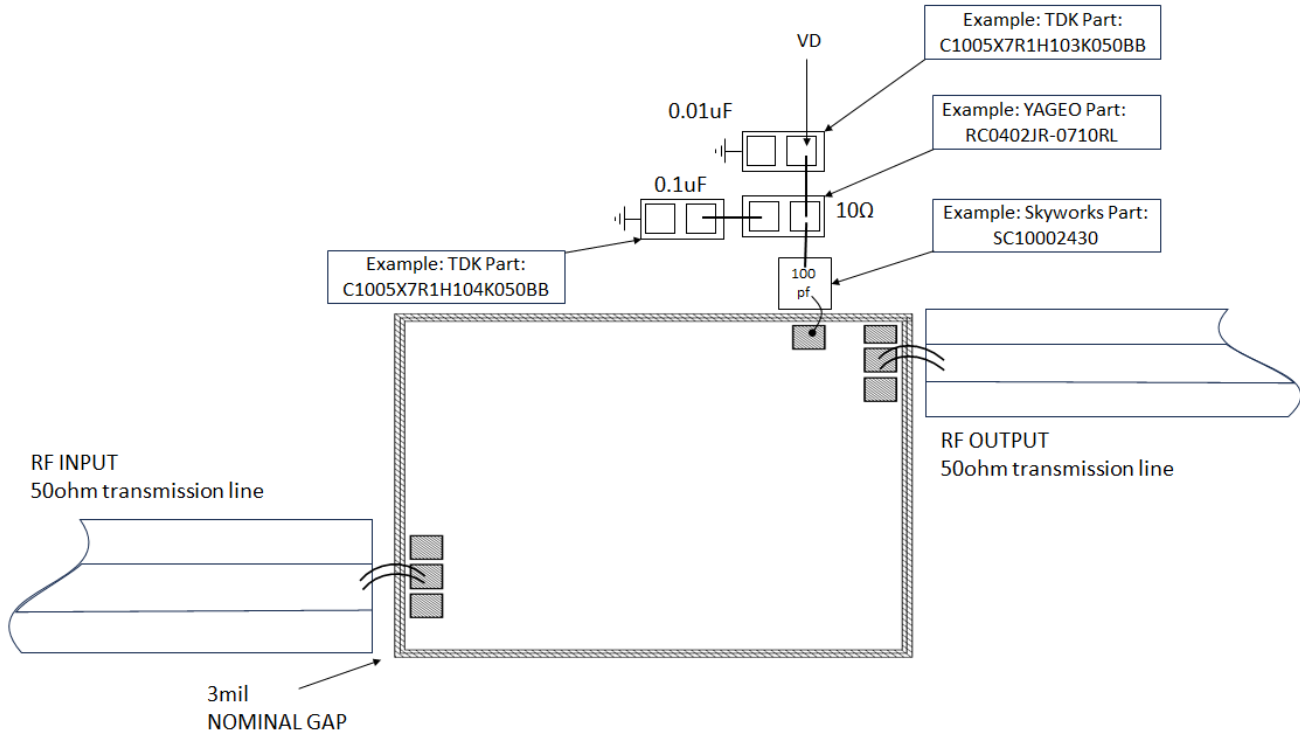


Notes:

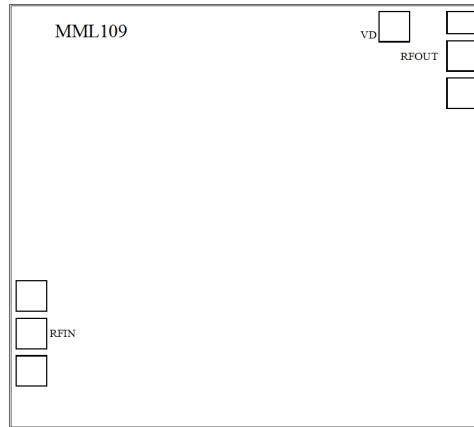
1. Die thickness: 100 μm
2. DC bond pad is 100*100 μm^2
3. RF IN/OUT bond pad is 100*100 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold



Assembly Drawing



No	Function	Description
1	RF IN	RF signal input terminal; blocking capacitor required.
2	RF OUT	RF signal output terminal; blocking capacitor required.
3	VD	Drain Biases for the Amplifier. Connect to external 100pf and 0.1uf bypass capacitors and 10Ω Resistors and 0.01uf capacitors.
4	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Apply positive drain voltage VD and set to +5V .
3. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Turn off the positive drain voltage VD.

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