

Features

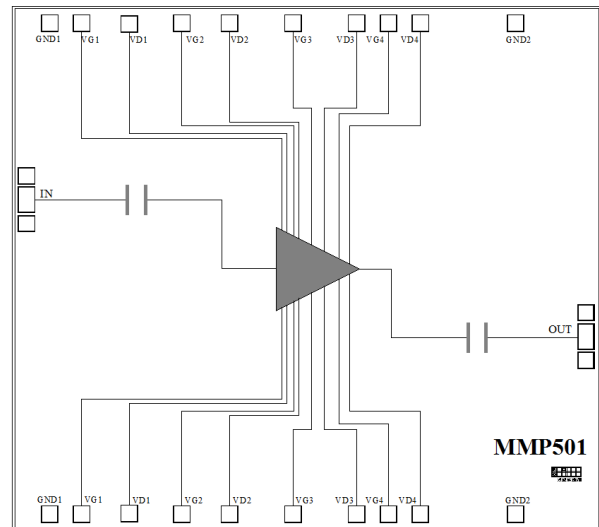
- Frequency: 18-44GHz
- Small Signal Gain: 21dB Typical
- Gain Flatness: ± 1.5 dB Typical
- Noise Figure: 4.5dB Typical
- Psat: 31dBm Typical @ +6V/-0.45V
- Supply voltage:
VD =+6V
VG=-0.45V

 Input/Output: 50 Ω

- Die Size: 3.7 x 3.3 x 0.1mm

Typical Applications

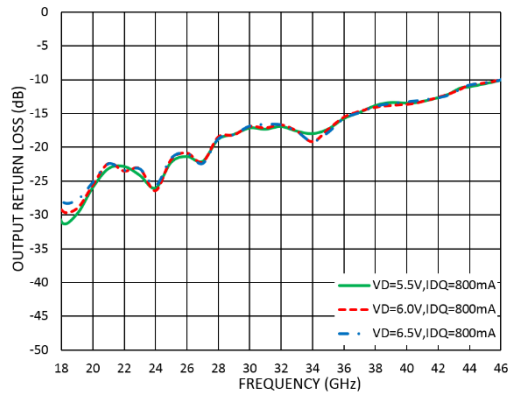
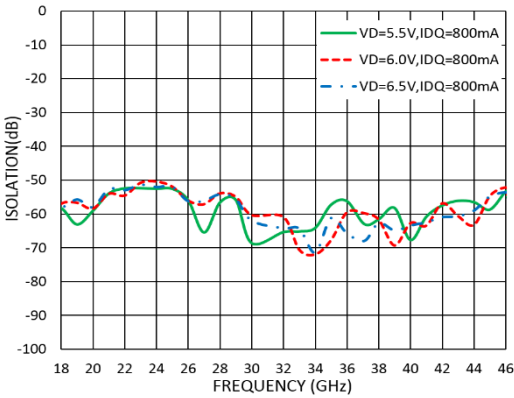
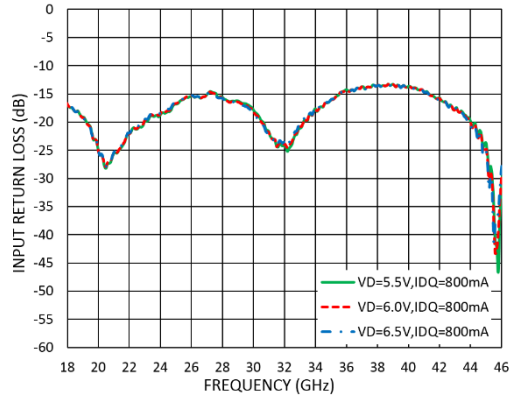
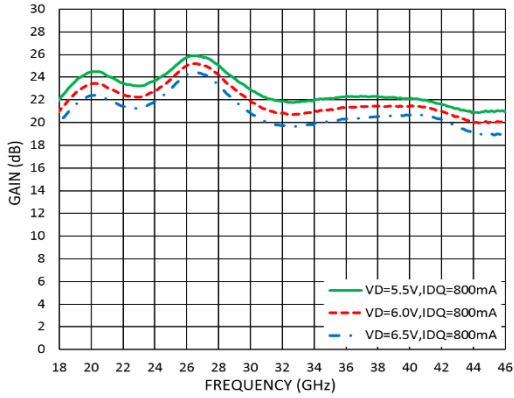
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

Electrical Specifications
TA = +25°C, VD=+6V, VG= -0.45V IDD = 800mA Typical

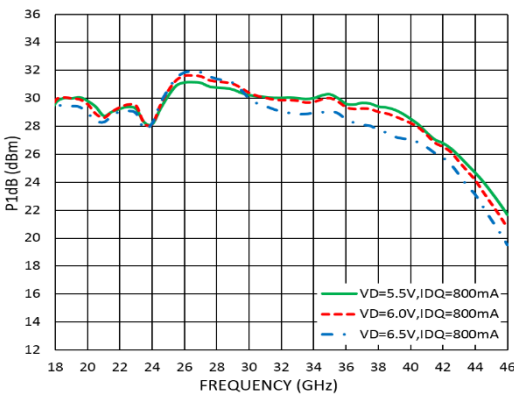
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	18-40		40-44				GHz
Small Signal Gain	20	23		18	21		dB
Gain Flatness		± 1.5			± 1.0		dB
Noise Figure		4.5			4.5		dB
P1dB - Output 1dB Compression	27	30		24	27		dBm
Psat - Saturated Output Power	28	31		25	28		dBm
Input Return Loss		15			15		dB
Output Return Loss		18			10		dB
* Adjust VG slightly to obtain device current of 800mA.							



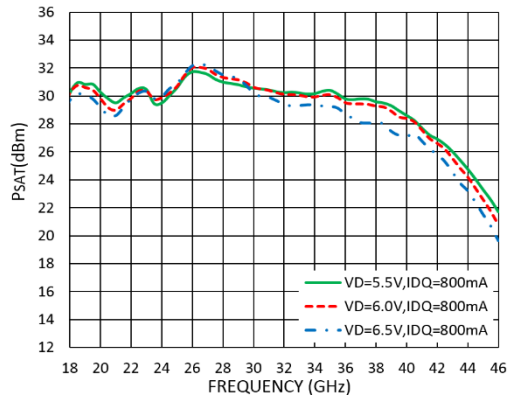
Measurement Plots: S-parameters



Measurement Plots: P1dB



Measurement Plots: PsAT





Absolute Maximum Ratings

Drain Bias Voltage (VD)	+8V
Gate Bias Voltages(VG)	-1 to 0 V
RF Input Power (RFIN)@(+6V)	+17dBm
Channel Temperature	175 °C
Continuous P _{diss} (T = 85 °C) (derate 89mW/°C above 85 °C)	8W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

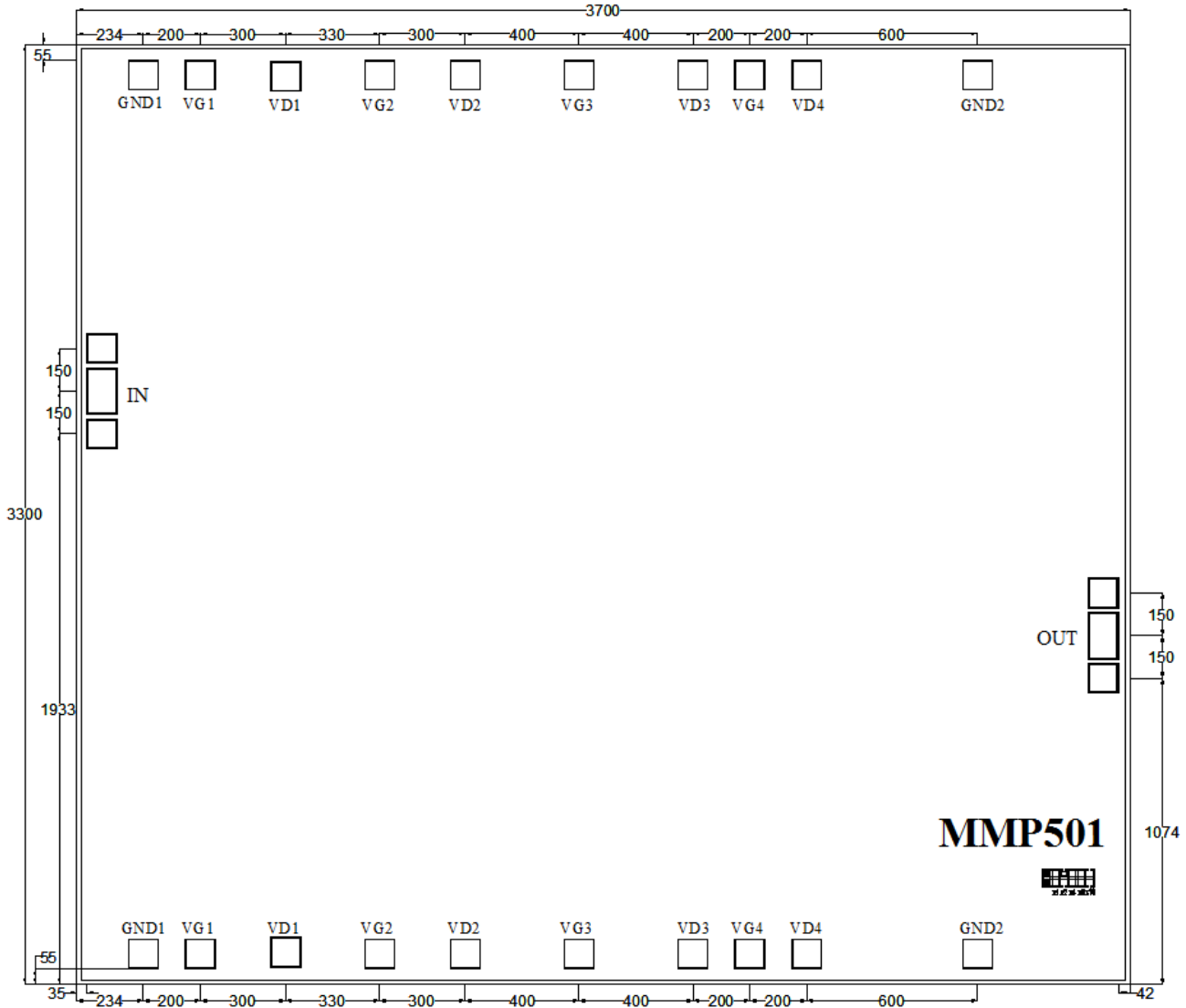
VD (V)	VG (V)	IDD (mA)
5.5	-0.36	800
6	-0.361	800
6.5	-0.383	800



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS



Outline Drawing: All Dimensions in μm

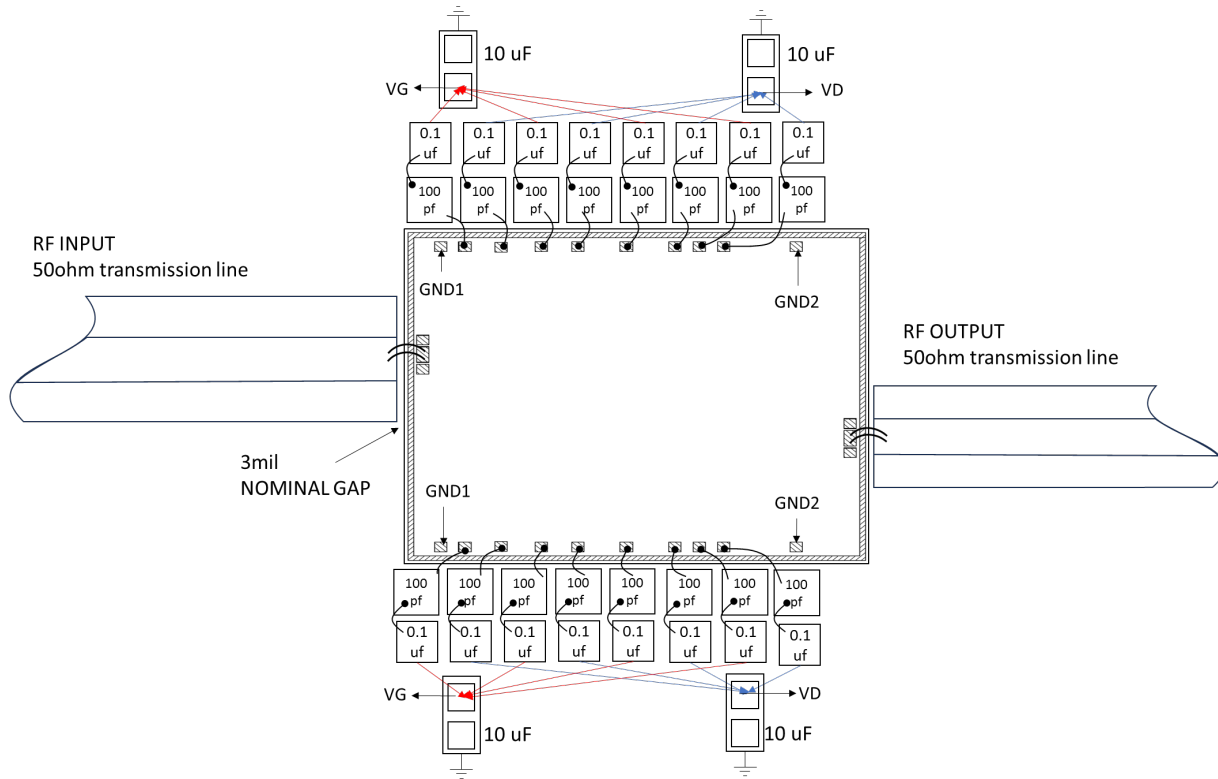


Notes:

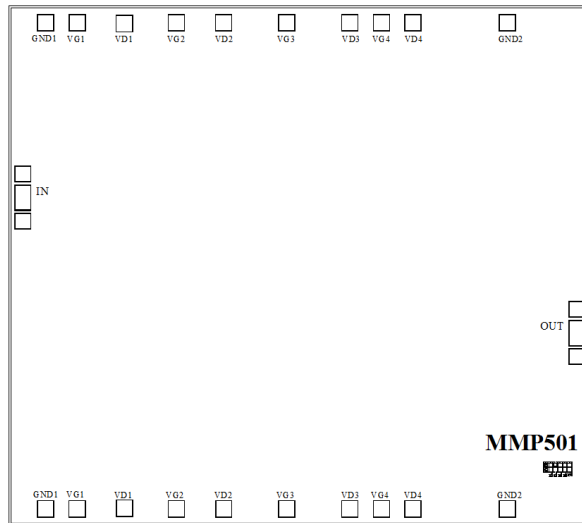
1. Die thickness: 100 μm
2. DC bond pad is 100*100 μm^2
3. RF IN/OUT bond pad is 100*100 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold



Assembly Drawing



No.	Mnemonic	Description
1	RF IN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
2	RF OUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
3	VG1&VG2&VG3&VG4	Amplifier Gate Controls. External bypass capacitors of 0.1 μf and 100 pf are required for these pads. ESD protection diodes are included and turn on below -1.0 V.
4	VD1&VD2&VD3&VD4	Drain Biases for the Amplifier. External bypass capacitors of 0.1 μf and 100 pf are required for these pads.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set all the gate bias voltages, VG1&VG2&VG3&VG4 ,to -1V.
3. Set all the drain bias voltages, VD1&VD2 &VD3&VD4 ,to +6 V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 800 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1&VG2&VG3&VG4, to -1V to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease all of the drain bias voltages to 0 V.
4. Increase the gate bias voltages to 0 V.

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