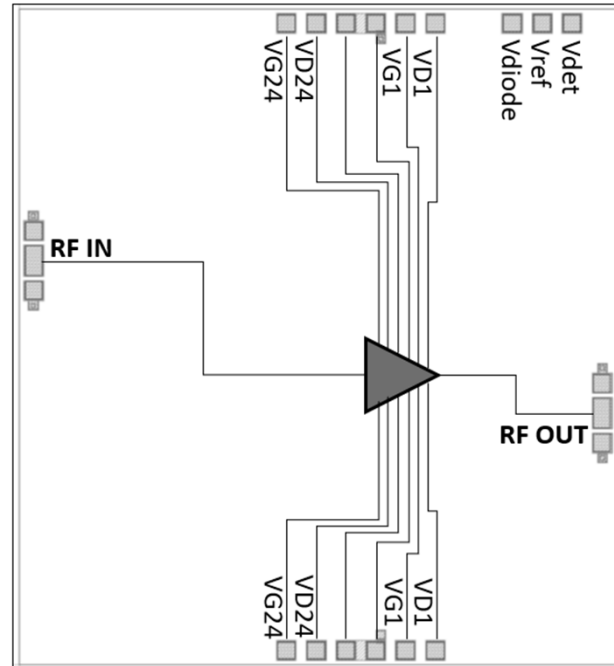


**Features**

- Frequency: 20GHz - 44GHz
- Small Signal Gain: 19dB
- Gain Flatness:  $\pm 2.0$ dB
- P1dB = 25 dBm to 26.5 dBm
- Power Supply: +6V/625mA
- Input/Output: 50 $\Omega$
- Die Size: 3.0 x 3.3 x 0.07 mm

**Typical Applications**

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

**Functional Block Diagram**

**Electrical Specifications**

TA = +25°C, VD1, VD24 = +6V, VG1, VG24 = -0.4V, ID1 = 337mA, ID24 = 288mA

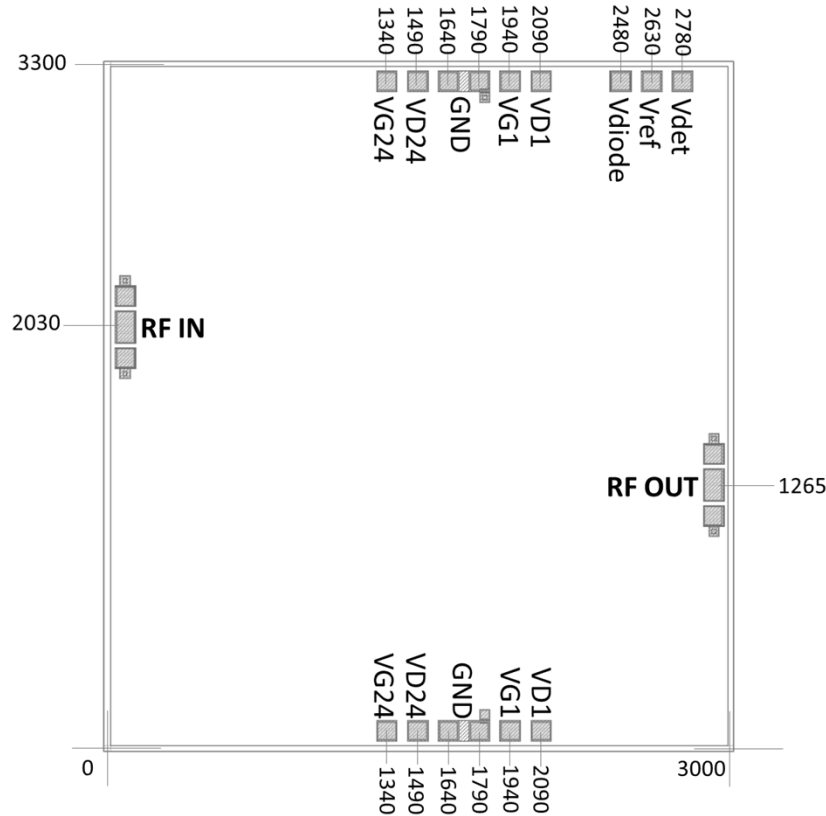
| Parameters                    | Min.    | Typ.    | Max. | Units |
|-------------------------------|---------|---------|------|-------|
| Frequency                     | 20 - 44 |         |      | GHz   |
| Small Signal Gain             |         | 19      |      | dB    |
| Gain Flatness                 |         | $\pm 2$ |      | dB    |
| Output 1dB Compression (P1dB) | 25.0    |         | 27.5 | dBm   |
| Saturated Output Power (Psat) | 26.7    |         | 28.9 | dBm   |
| Input Return Loss             |         | > 10    |      | dB    |
| Output Return Loss            |         | > 10    |      | dB    |

\* Adjust VG1, VG24 slightly to obtain total drain currents of 630 mA.



### Outline Drawing:

All Dimensions in  $\mu\text{m}$

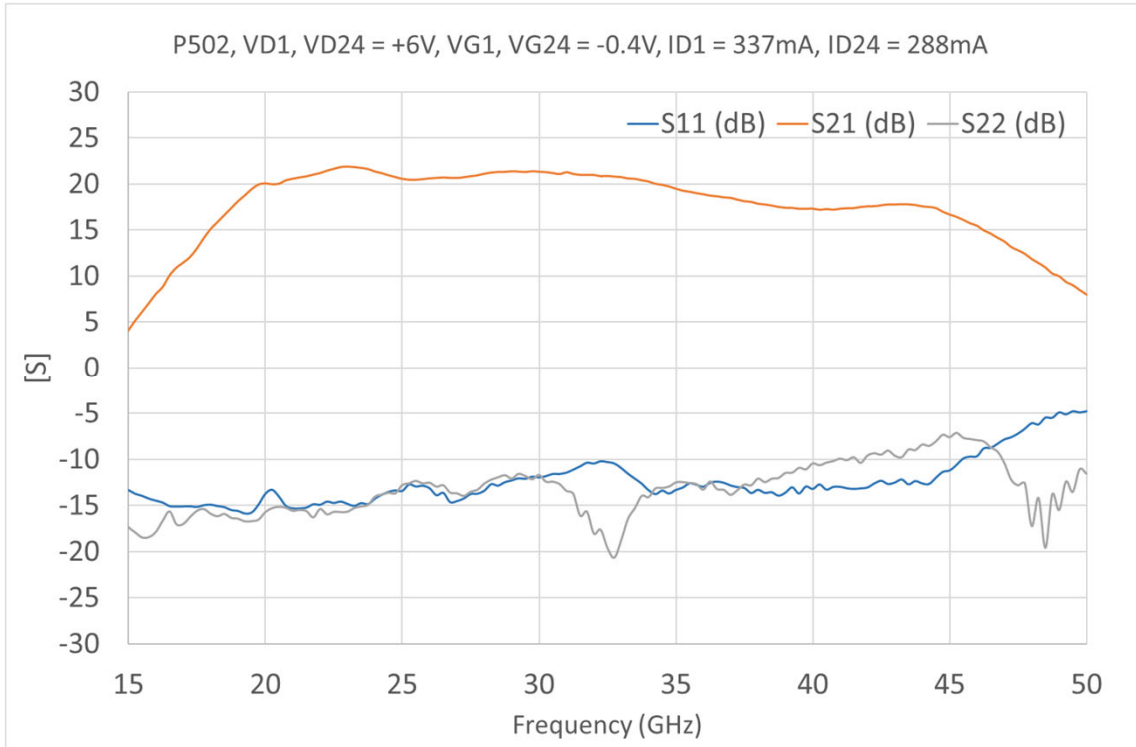


### Pad Description

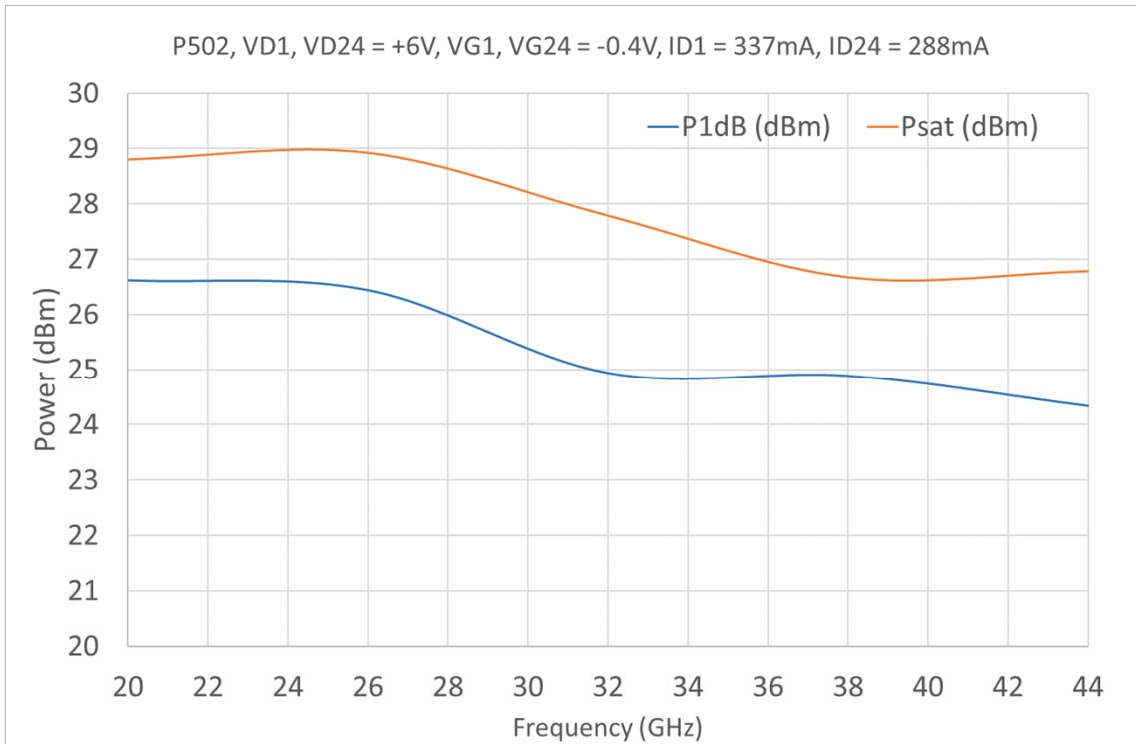
| No | Function  | Description  |
|----|-----------|--|
| 1  | RF IN     | Signal input terminal, connected to 50 $\Omega$ circuit                        |
| 2  | RF OUT    | Signal output terminal, connected to 50 $\Omega$ circuit                       |
| 3  | VG1, VG24 | Amplifier gate bias; connect to external 1000pF and 0.01uF bypass capacitors.  |
| 4  | VD1, VD24 | Amplifier drain bias; connect to external 1000pF and 0.01uF bypass capacitors. |
| 5  | Vdiode    | Diode biasing voltage  |
| 6  | Vref      | Reference diode output voltage   |
| 7  | Vdet      | Detector output voltage  |
| 8  | GND       | Ground pads  |



### Measurement Plots: S-parameters

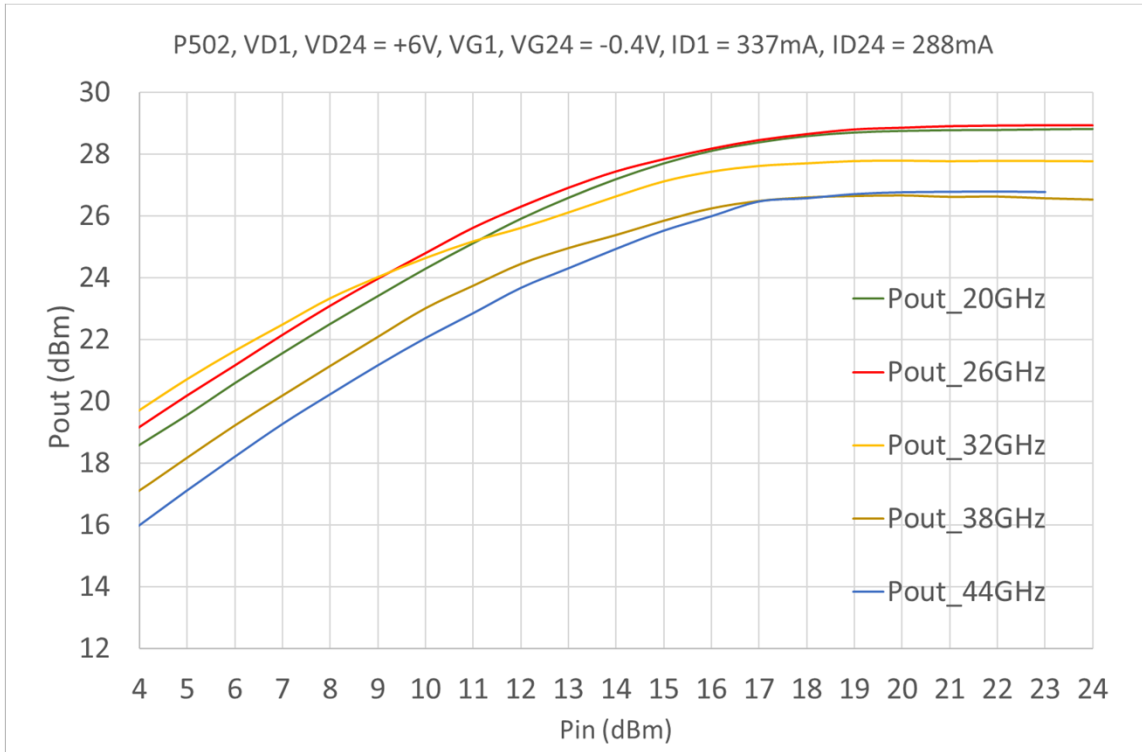


### Measurement Plots: P1dB and Psat

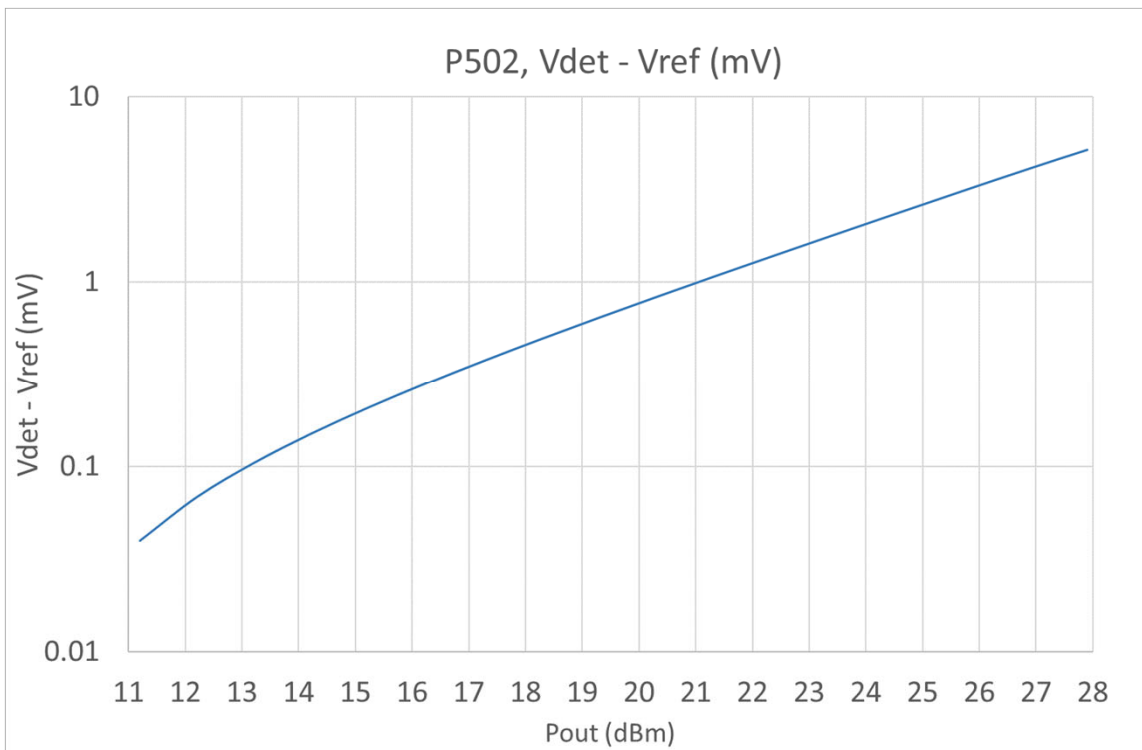




### Measurement Plots: Pout vs Pin

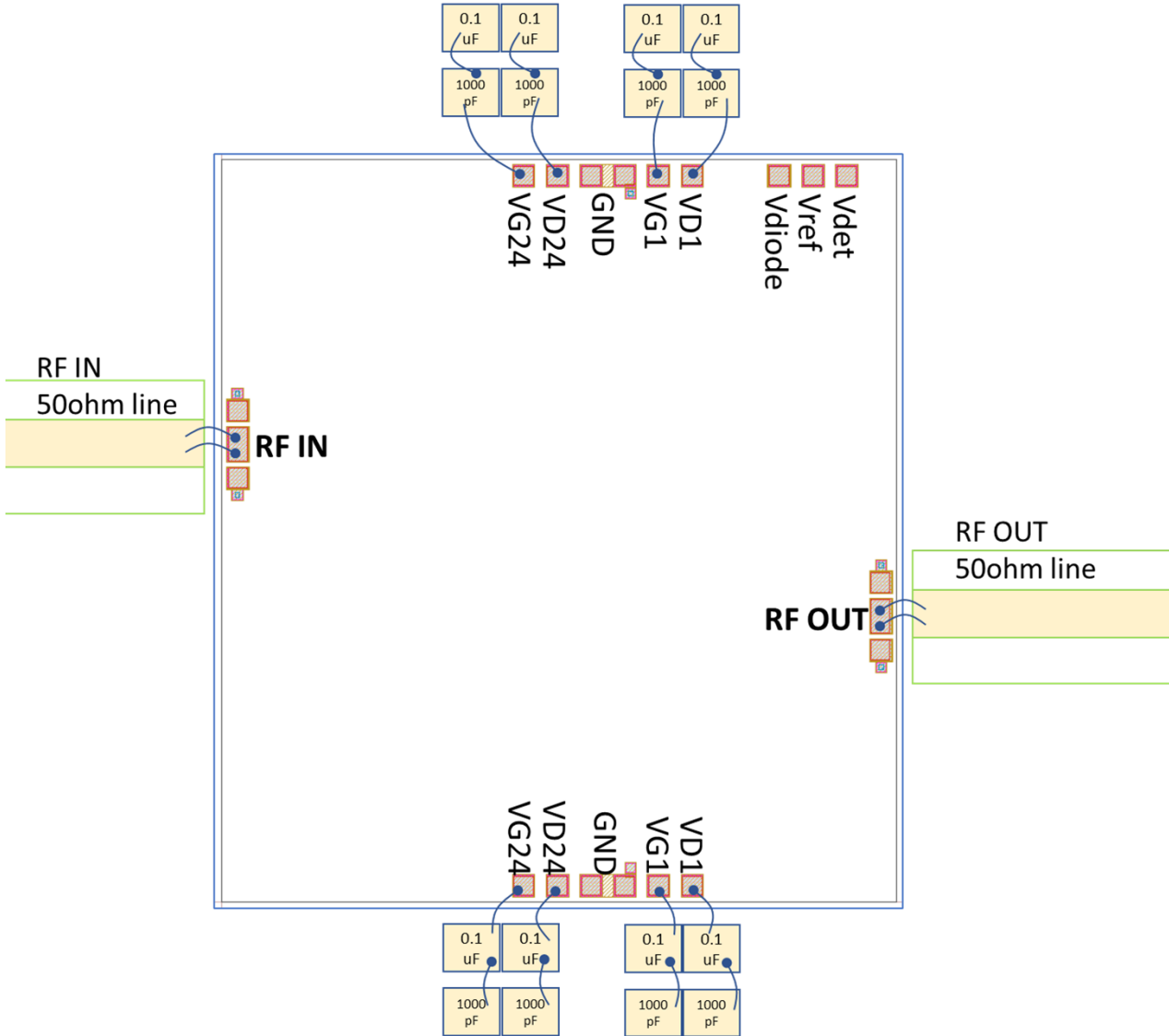


### Measurement Plots: Vdet - Vref





### Assembly Drawing



#### Notes:

1. Die thickness: 70um
2. DC bond pad is 100 x 100  $\mu\text{m}^2$
3. RF IN/OUT bond pad is 100 x 160  $\mu\text{m}^2$
4. Bond pad metalization: Gold
5. Backside metalization: Gold
6. Backside of the die (GND)