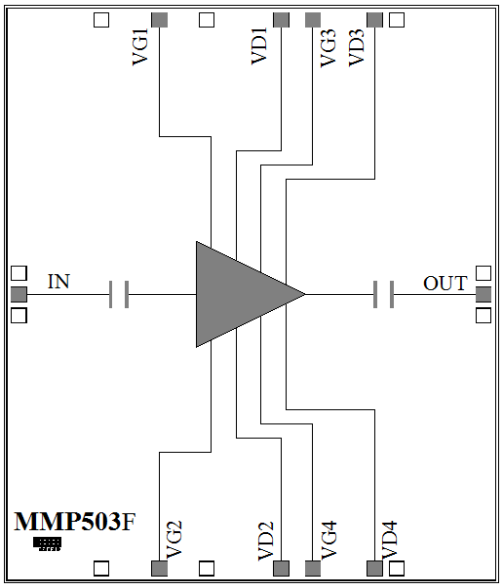
Features

- Frequency: 18 - 44GHz
- Small Signal Gain: 26dB Typical
- Gain Flatness: ±1.5dB Typical
- Noise Figure: 6dB Typical
- P1dB: 30dBm Psat: 31dBm Typical @ +5V/-0.4V
- Supply voltage:
  VD =+4.5V to +5.5V
  VG=-0.3V to -0.4V
- Input/Output: 50Ω
- Die Size: 3.4 x 4.1 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

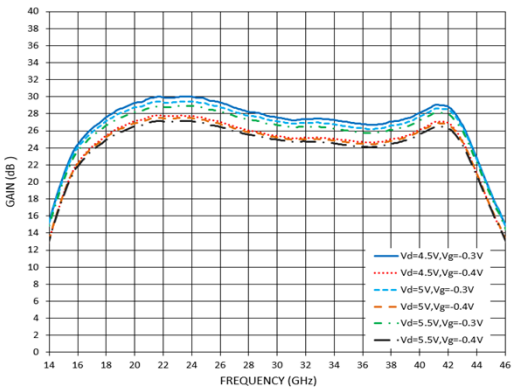


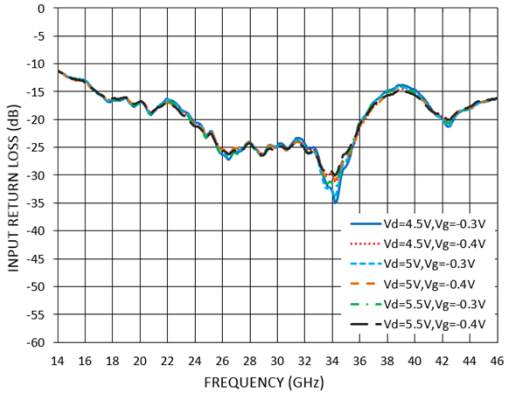
Electrical Specifications

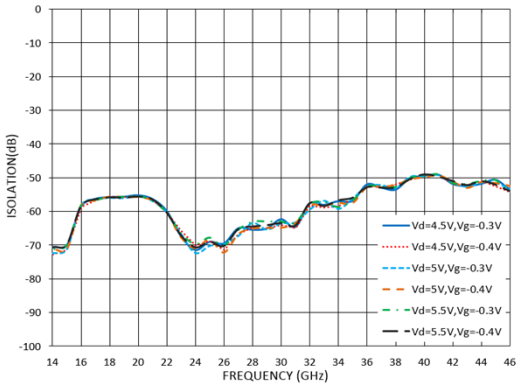
TA = +25°C, VD=+5V,VG= -0.4V IDD = 1400mA Typical

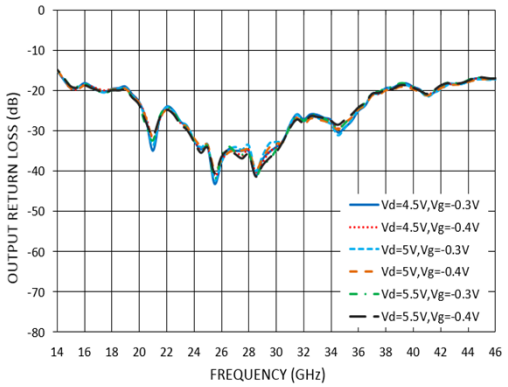
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	18-28			28-38			38-44			GHz
Small Signal Gain	24	26		24	25		20	24		dB
Gain Flatness		±2.0			±1.0			±3.0		dB
Noise Figure		6			5.8			6.5		dB
P1dB - Output 1dB Compression		30			30			29		dBm
Past - Saturated Output Power		32			31			30		dBm
Input Return Loss		18			18			18		dB
Output Return Loss		20			20			20		dB
* Adjust VG slightly to obtain device current of 1400 mA.										

Measurement Plots: S-parameters

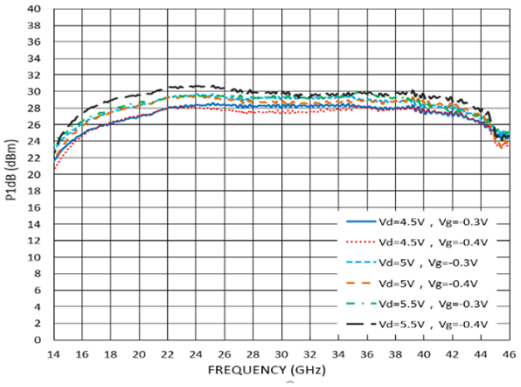




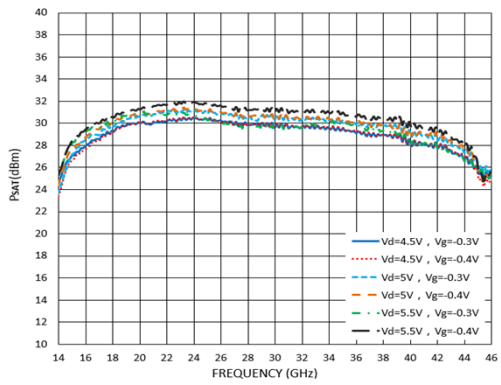




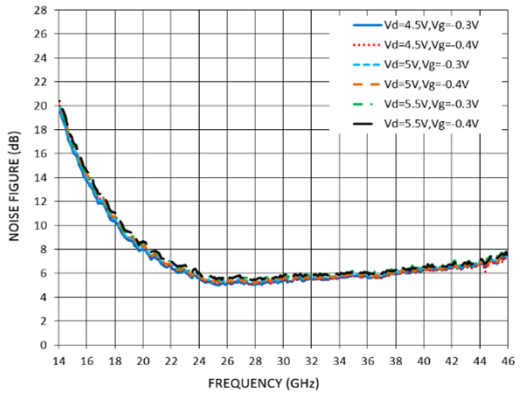
Measurement Plots: P1dB



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+6V
Gate Bias Voltages(VG)	–1.5 to 0 V
RF Input Power (RFIN)	+15dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 155mW/°C above 85 °C)	14W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-55°C to +150 °C

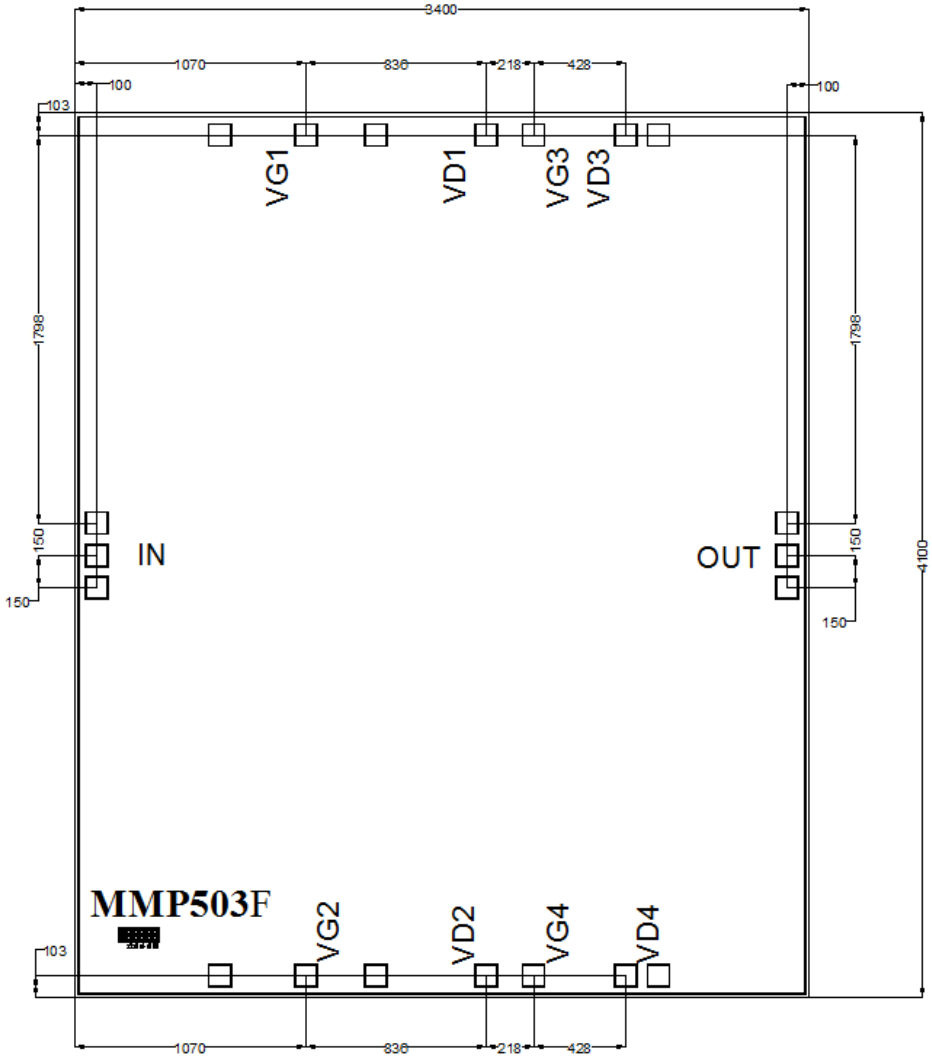
Typical Supply Current vs. VD,VG

VD (V)	VG (V)	IDD (mA)
4.5	-0.3	1677
4.5	-0.4	1266
5.5	-0.3	1929
5.5	-0.4	1550
5	-0.3	1808
5	-0.4	1394

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:

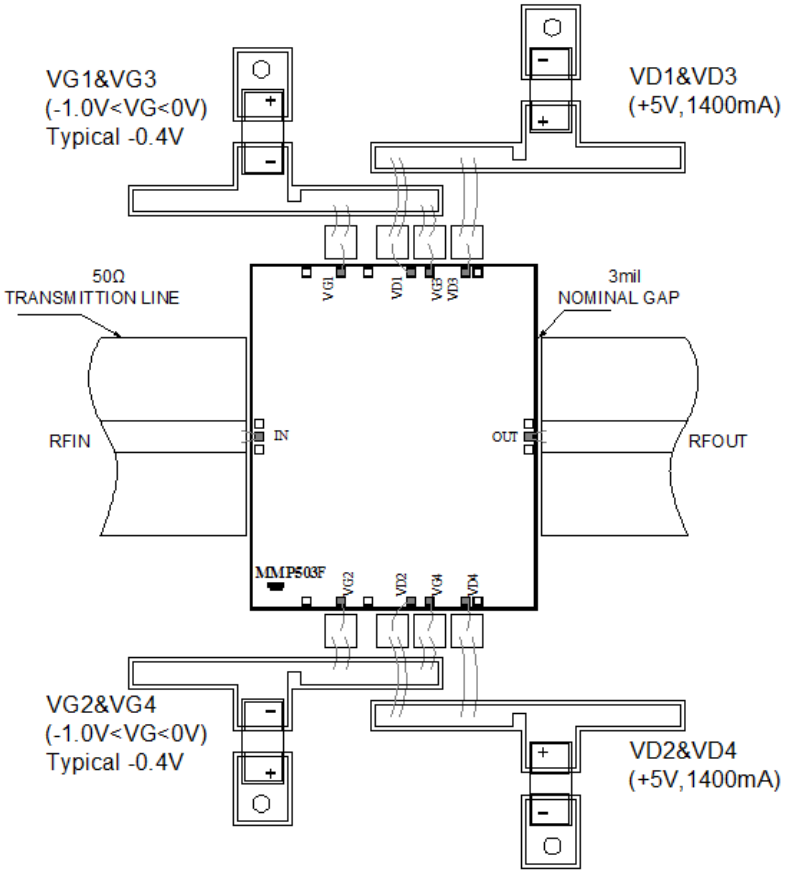
All Dimensions in µm



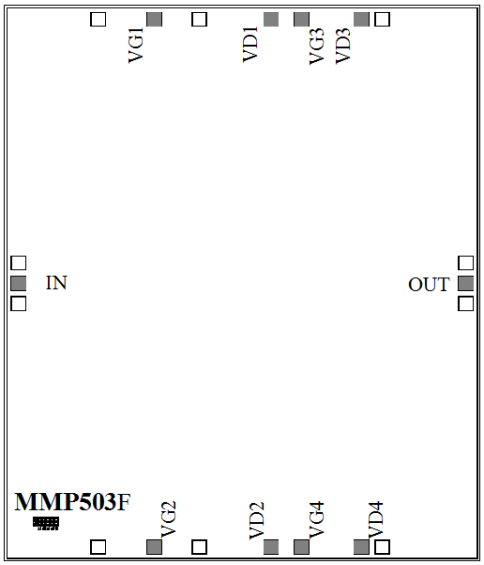
Notes:

1. **Die thickness: 100µm**
2. **DC bond pad is 100 x 100 µm^2**
3. **RF IN/OUT bond pad is 100 x 100 µm^2**
4. **DC bond pad is 100 x 100 µm^2**
5. **Bond pad metalization: Gold**
6. **Backside metalization: Gold**
7. **Backside of the die (GND)**

Assembly Drawing



No.	Mnemonic	Description
1	RF IN	RF Signal Input. This pad is ac-coupled and matched to 50 Ω.
2	RF OUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
3	VG1&VG3 OR VG2&VG4	Amplifier Gate Controls. External bypass capacitors of 10 µF and 1000 pF are required for these pads. ESD protection diodes are included and turn on below −1.0 V.
4	VD1&VD3 OR VD2&VD4	Drain Biases for the Amplifier. External bypass capacitors of 10 µF and 1000 pF are required for these pads.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set all the gate bias voltages, VG1&VG3 OR VG2&VG4 ,to −1.0V.
3. Set all the drain bias voltages, VD1&VD3 OR VD2&VD4 ,to +5 V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 1400 mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1&VG3 OR VG2&VG4, to −1.0V to achieve a I_{DQ} = 0 mA (approximately).
3. Decrease all of the drain bias voltages to 0 V.
4. Increase the gate bias voltages to 0 V.