

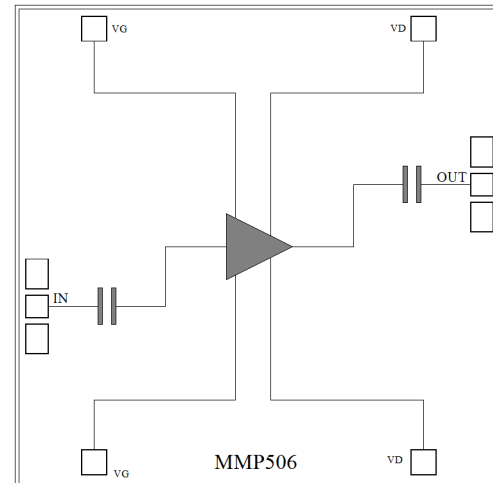
### Features

- Frequency: 25-65GHz
- Small Signal Gain: 25dB Typical
- Gain Flatness:  $\pm 1.5$ dB Typical
- Noise Figure: 3.6dB Typical
- Psat: 22dBm Typical
- Power Supply:  
VD=+4V@173mA, VG=-0.3V
- Input/Output: 50 $\Omega$
- Die Size: 2.02 x 2.0 x 0.05mm

### Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

### Functional Block Diagram



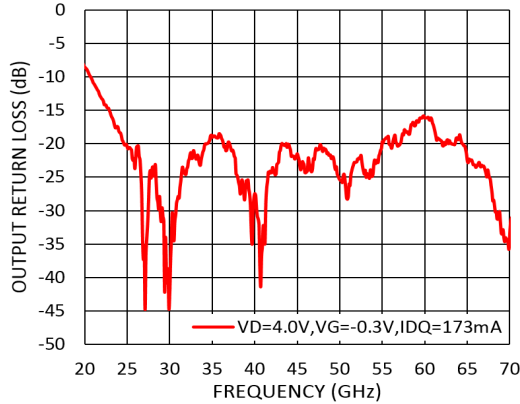
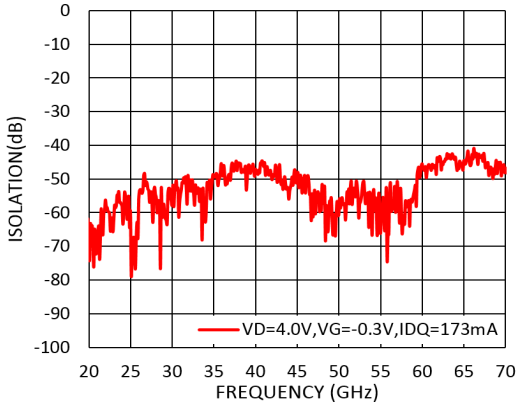
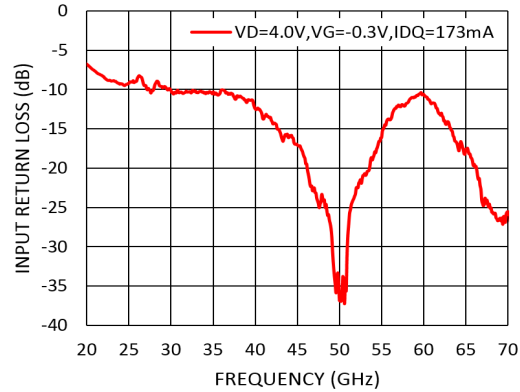
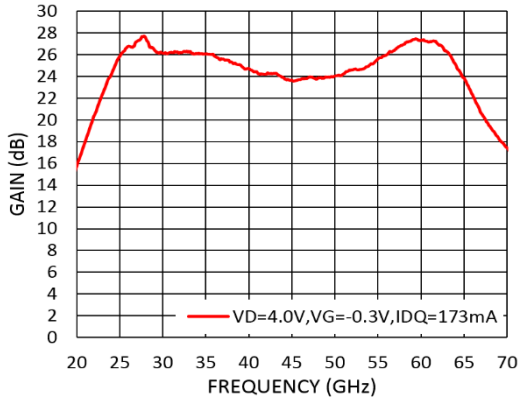
### Electrical Specifications

TA = +25°C, VD=+4V, VG= -0.3V IDD = 173mA Typical

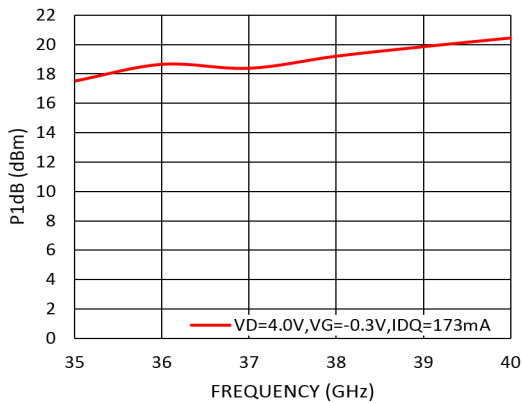
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	25 - 40			40 - 65			GHz
Small Signal Gain	23	25		22	25		dB
Gain Flatness		$\pm 0.5$			$\pm 1.5$		dB
Noise Figure		3.6			4.0		dB
P1dB - Output 1dB Compression		18			21		dBm
Psat - Saturated Output Power		22			23		dBm
OIP3 - Output Third Order Intercept		28			31		dBm
Input Return Loss		-10			-13		dB
Output Return Loss		-20			-17		dB



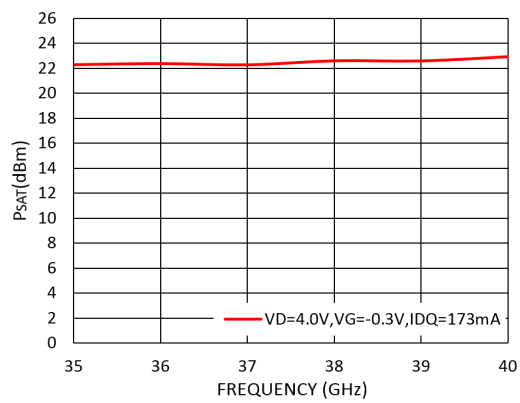
### Measurement Plots: S-parameters

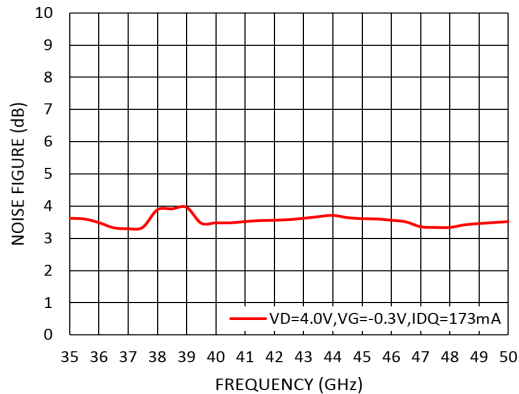


### Measurement Plots: P1dB



### Measurement Plots: PSAT



**Measurement Plots: Noise Figure**

**Absolute Maximum Ratings**

Drain Bias Voltage (VD)	+4.5V
Gate Bias Voltage (VG)	-2V to 0V
RF Input Power (RFIN)@(+4V)	+15dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 9mW/°C above 85 °C)	0.81W
Thermal Resistance (channel to die bottom)	26°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

**Typical Supply Current vs. VD,VG**

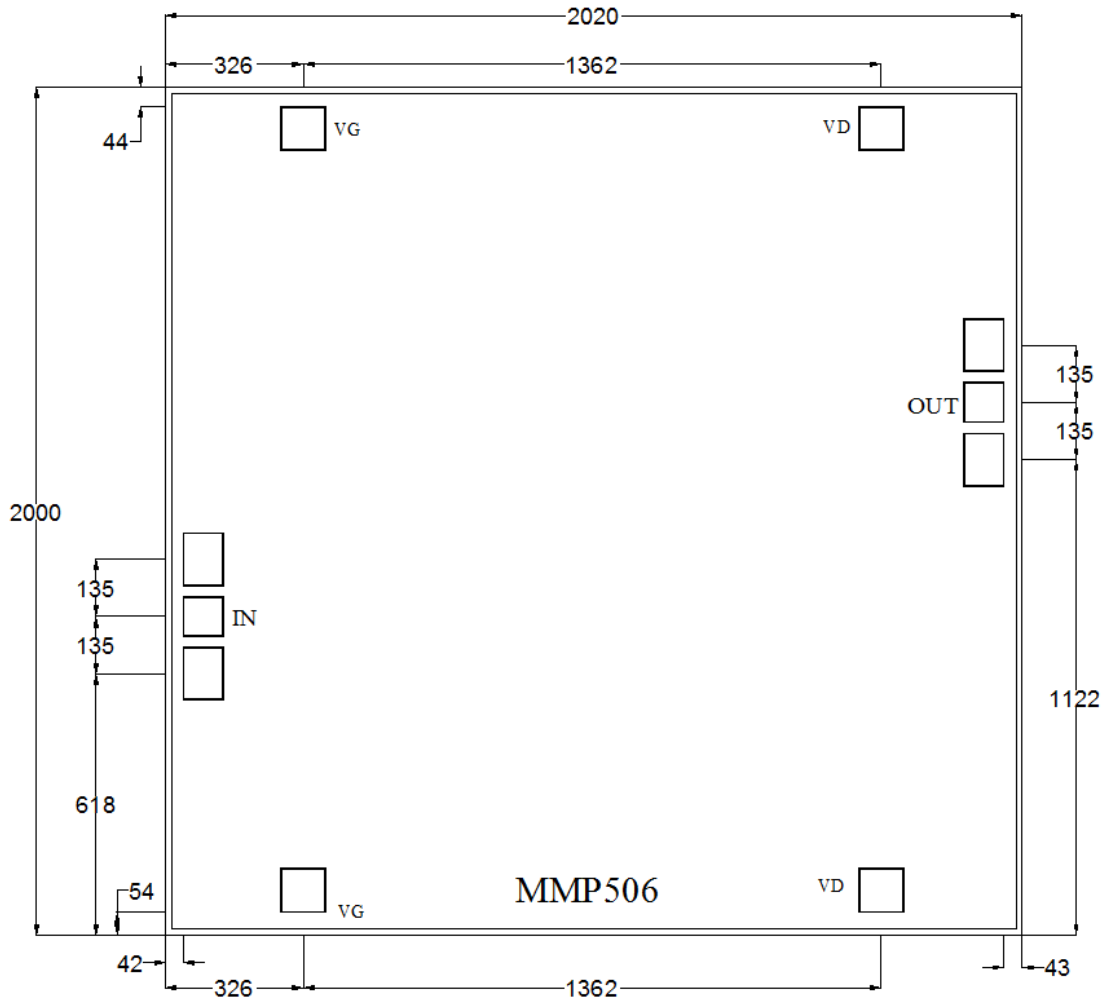
VD (V)	VG (V)	IDD (mA)
+4	-0.3	173



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**



### Outline Drawing: All Dimensions in $\mu\text{m}$

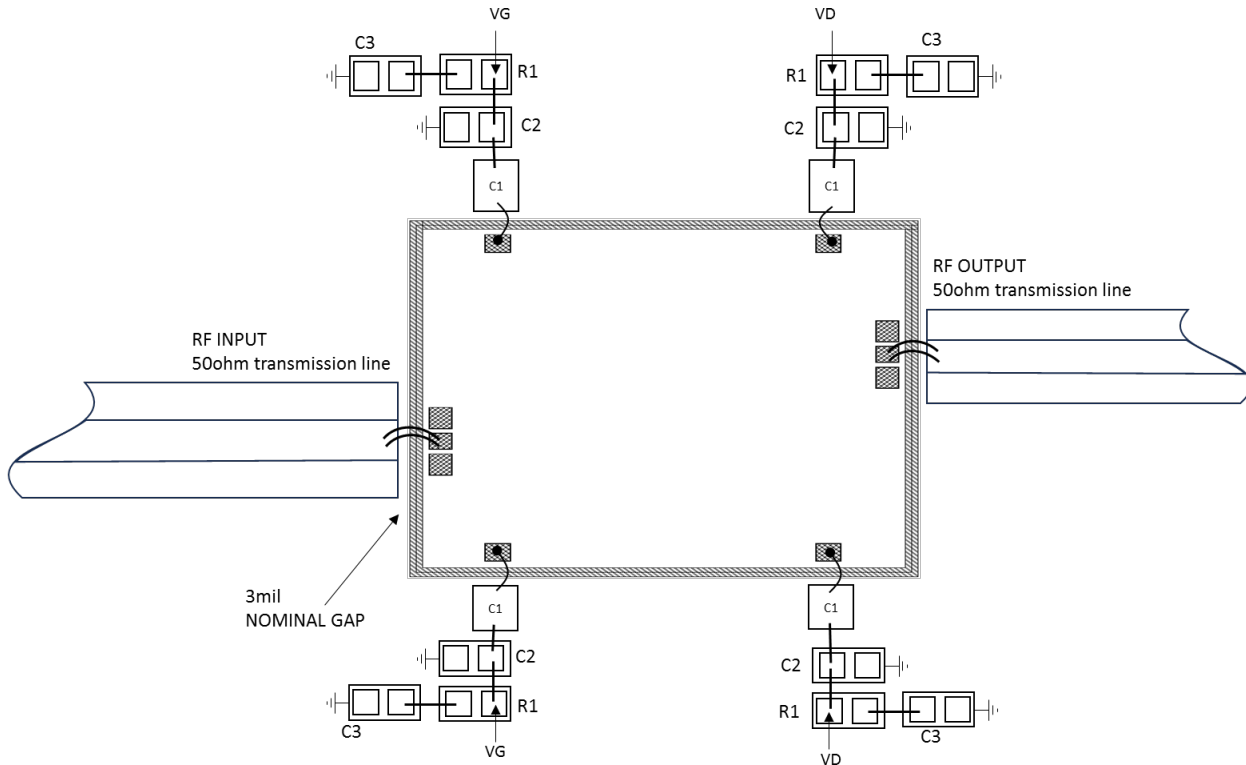


#### Notes:

1. Die thickness: 50 $\mu\text{m}$
2. VD bond pad is 100\*100 $\mu\text{m}^2$
3. VG bond pad is 100\*100 $\mu\text{m}^2$
4. RF IN/OUT bond pad is 90\*90 $\mu\text{m}^2$
5. Bond pad metalization: Gold
6. Backside metalization: Gold

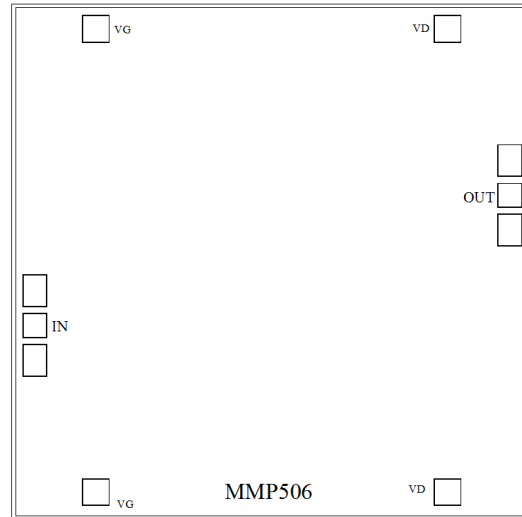


### Assembly Drawing



Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1
C2	0.01 $\mu$ F Example: TDK Part: C1005X7R1H103K050BB (0402)
C3	0.1 $\mu$ F Example: Murata Electronics Part: GRM033Z71C104KE14D (0201)
R1	10 $\Omega$ Example: Yageo Part: RC0201FR-0710RP

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



## Biasing and Operation

### Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VG to  $-2V$ .
3. Set the drain bias voltages VD to  $+4V$ .
4. Increase the gate bias voltages to achieve a quiescent supply current of 173 mA.
5. Apply RF signal.

### Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG to  $-2V$  to achieve a  $I_{DQ} = 0$  mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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