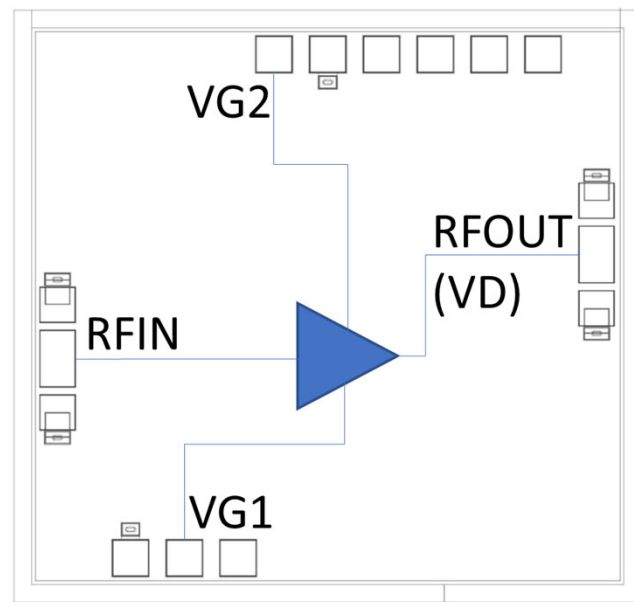


Features

- Frequency: DC-65GHz
- Small Signal Gain: >12 dB
- Gain Flatness: $\leq \pm 1.0$ dB@ 5-65GHz
- Noise Figure: <4 dB@35GHz
- P1dB = 13 dBm@35GHz
- Psat = 16.5 dBm@35GHz
- Power Supply: +4.5V/81mA
- Input/Output: 50Ω
- Die Size: 1.6 x 1.7 x 0.05 mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

Electrical Specifications

TA = +25°C, VD = +4.5V, VG1 = -0.35V, VG2 = 1.9V, ID = 81mA

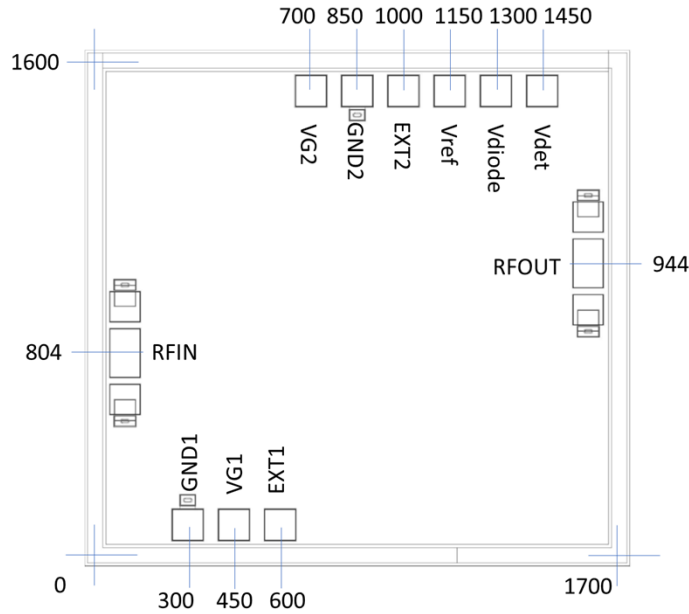
| Parameters | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|--------------------------------------|-------------|-----------|------|-------------|-----------|------|--------------|---------|------|------------|
| Frequency | DC-5 | | | 5-55 | | | 55-65 | | | GHz |
| Small Signal Gain | 12.5 | 15 | 14.7 | 11.5 | 12 | 12.5 | 11 | 12 | 12.5 | dB |
| Gain Flatness | | ± 1.5 | | | ± 0.5 | | | ± 1 | | dB |
| Noise Figure | | 5 | | 3 | | 5 | 4.5 | | 6.5 | dB |
| Output 1dB Compression (P1dB) | 14.5 | | 15 | 12 | | 15 | 10 | | 12 | dBm |
| Saturated Output Power (Psat) | 18 | | 18.5 | 17 | | 18.5 | 13 | | 15 | dBm |
| Input Return Loss | < 15 | | | < 10 | | | < 8 | | | dB |
| Output Return Loss | < 10 | | | < 10 | | | < 10 | | | dB |

* Adjust VG1, VG2 slightly to obtain device current of 81mA.



Outline Drawing:

All Dimensions in μm

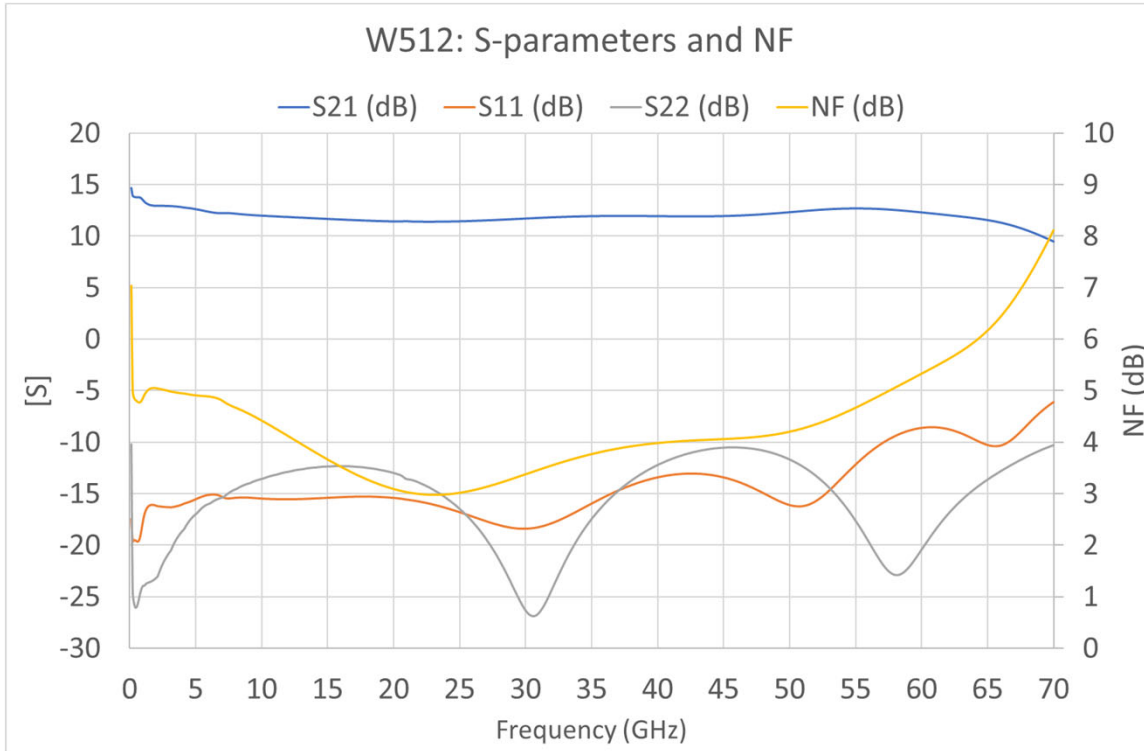


Pad Description

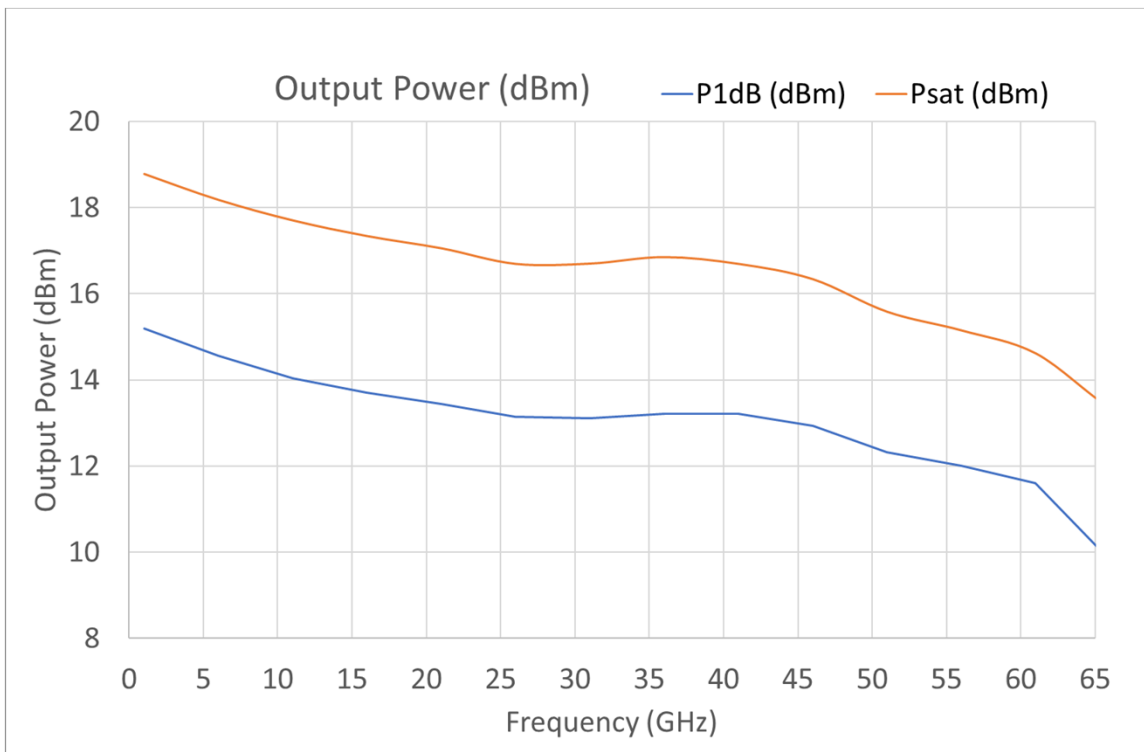
| No | Function | Description |
|----|------------|--|
| 1 | RF IN | Signal input terminal, connected to 50 Ω circuit, DC-coupled |
| 2 | RF OUT | Signal output terminal, connected to 50 Ω circuit; blocking capacitor required; external DC biasing network required. |
| 3 | VG1 | Amplifier 1 st gate bias; connect to external 1000pF and 0.01uF bypass capacitors. |
| 4 | VG2 | Amplifier 2 nd gate bias; connect to external 1000pF and 0.01uF bypass capacitors. |
| 5 | EXT1 | External bypass pad; connect to external bypass capacitors. |
| 6 | EXT2 | External bypass pad; connect to external bypass capacitors. |
| 7 | Vdiode | Diode biasing voltage |
| 8 | Vref | Reference diode output voltage |
| 9 | Vdet | Detector output voltage |
| 10 | GND1, GND2 | Ground pads. |



S-parameters and NF

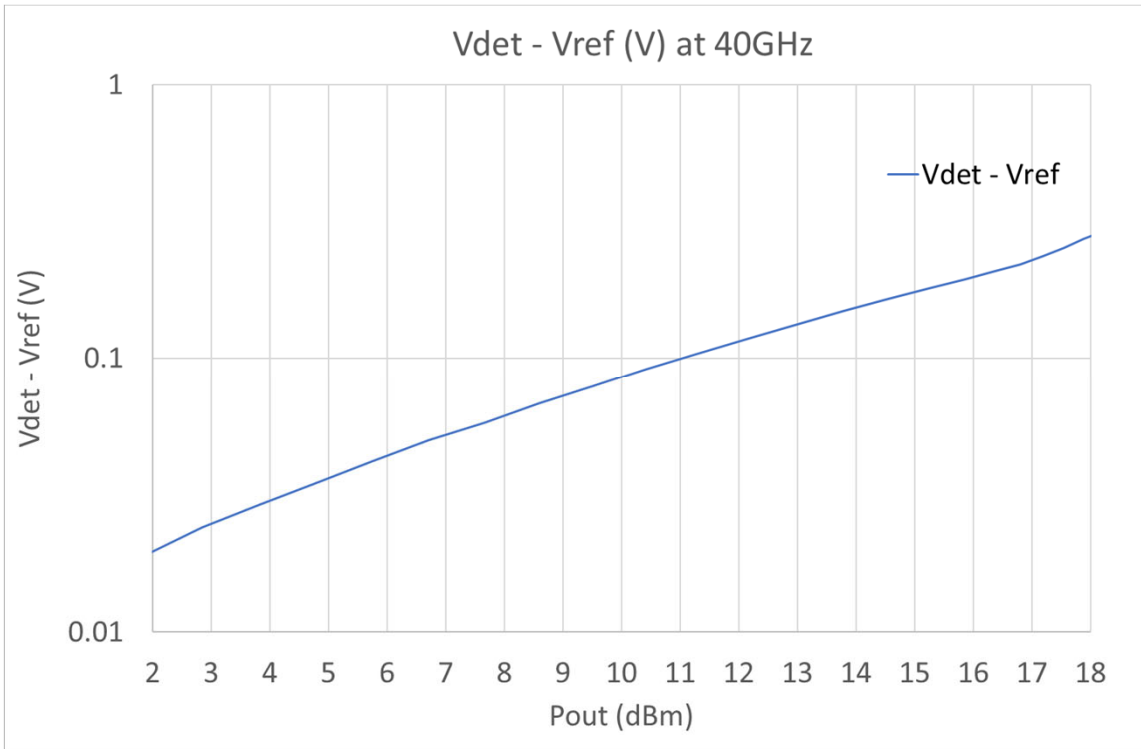


P1dB and Psat

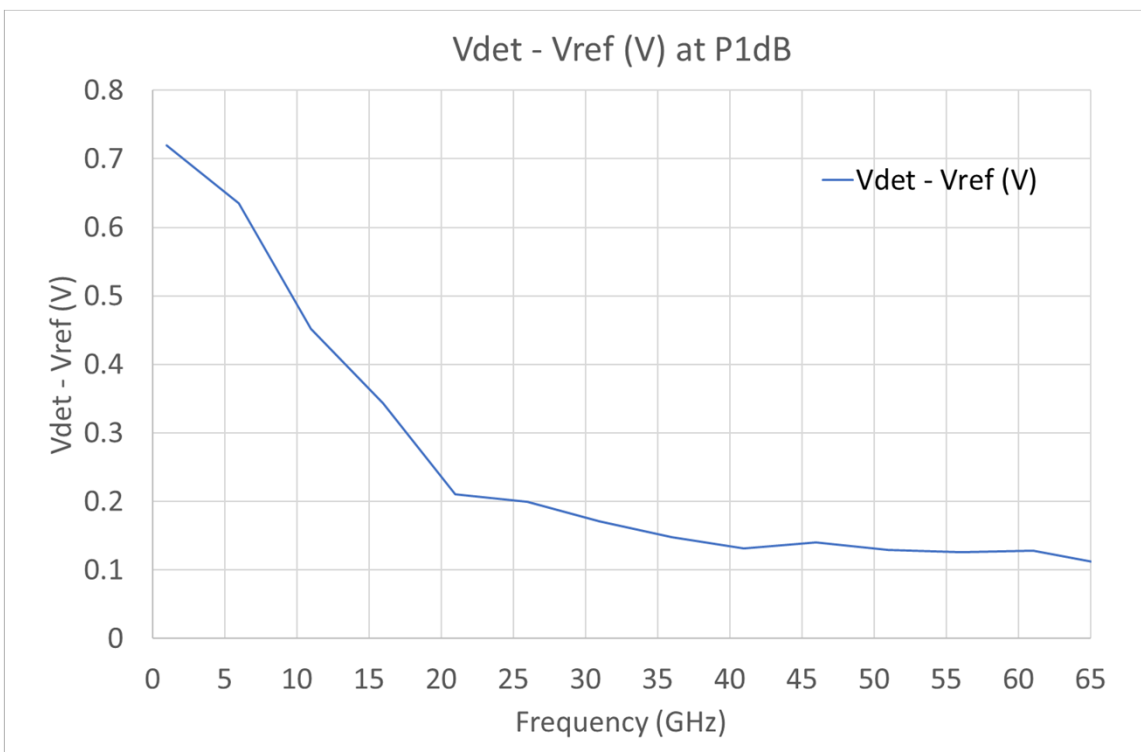




Power Detection: $V_{det} - V_{ref}$ vs P_{out} at 40GHz, $V_{diode} = 1V$

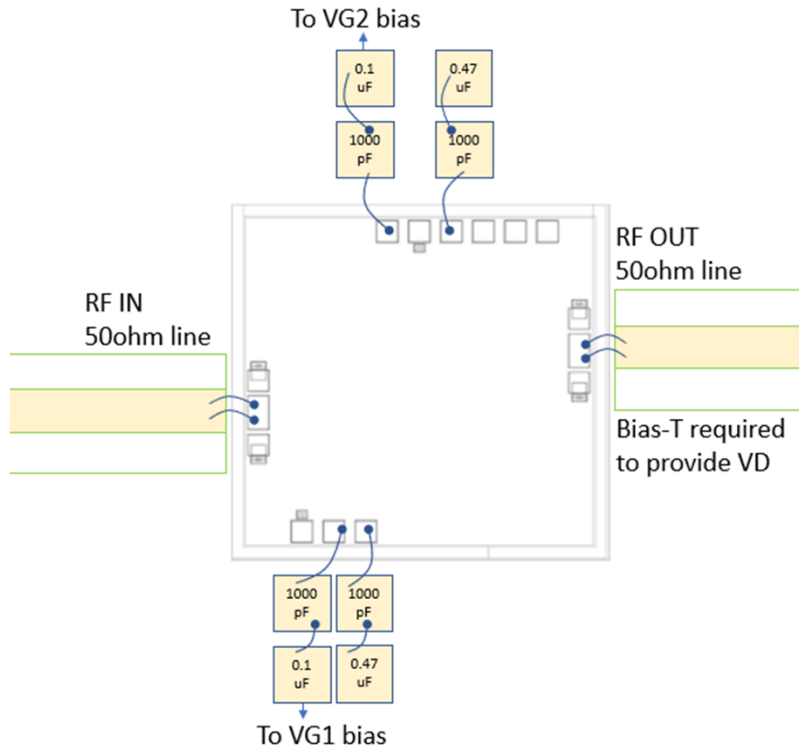


Power Detection: $V_{det} - V_{ref}$ vs Frequency at P1dB, $V_{diode} = 1V$





Assembly Drawing



Notes:

1. Die thickness: 50um
2. DC bond pad is 100 x 100 μm^2
3. RF IN/OUT bond pad is 100 x 160 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold
6. Backside of the die (GND)