

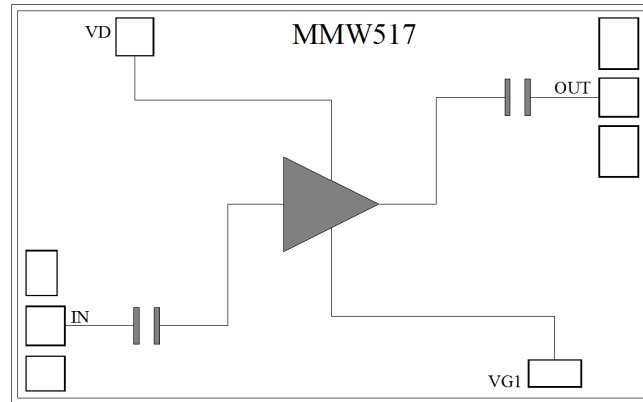
Features

- Frequency: 0.5-65GHz
- Small Signal Gain: 11dB Typical
- Gain Flatness: ± 2.0 dB Typical
- Noise Figure: 3.5dB Typical
- P1dB: 19dBm Typical
- Psat: 22dBm Typical
- Power Supply:
VD = +8V@86mA, VG1 = -1.5V
- Input/Output: 50 Ω
- Die Size: 1.6 x 1.0 x 0.05mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram



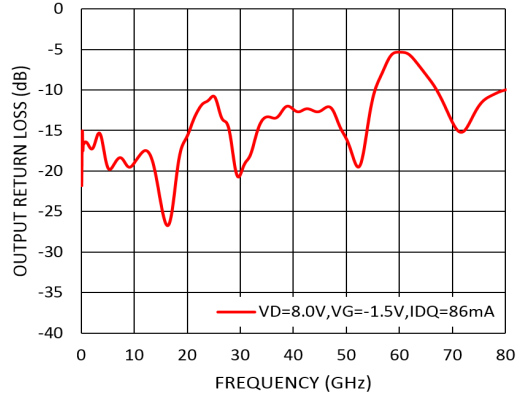
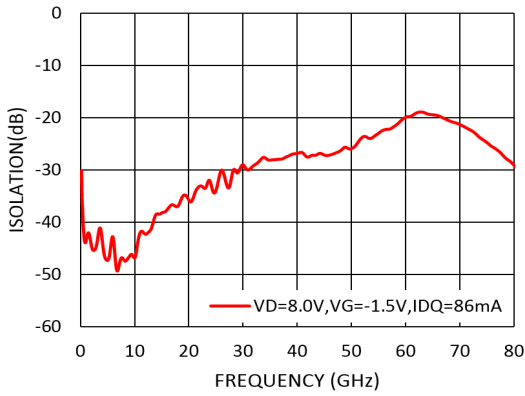
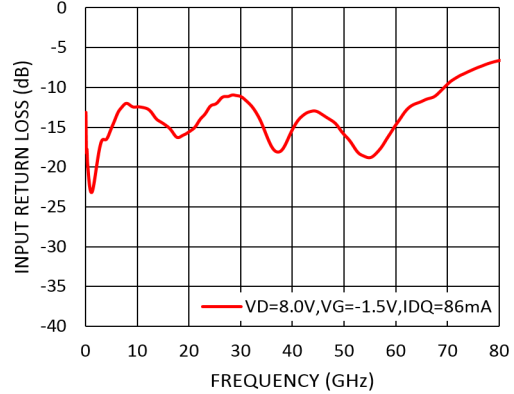
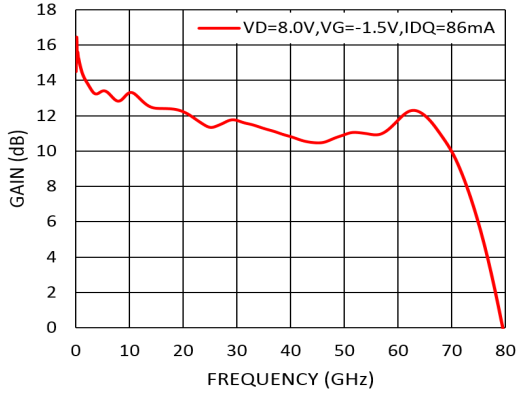
Electrical Specifications

TA = +25°C, VD=+8V, VG1= -1.5V IDD = 86mA Typical

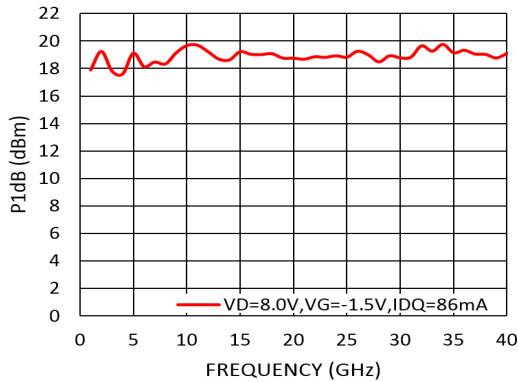
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	0.5 -20			20-50			50 - 65			GHz
Small Signal Gain	11	12.5		10	11		10	11		dB
Gain Flatness		± 2.0			± 0.5			± 1.0		dB
Noise Figure		3.5			4.5			6.0		dB
P1dB - Output 1dB Compression		19			19			18		dBm
Psat - Saturated Output Power		22			21			20		dBm
OIP3 - Output Third Order Intercept		28			27			26		dBm
Input Return Loss		-13			-12			-12		dB
Output Return Loss		-16			-12			-7		dB



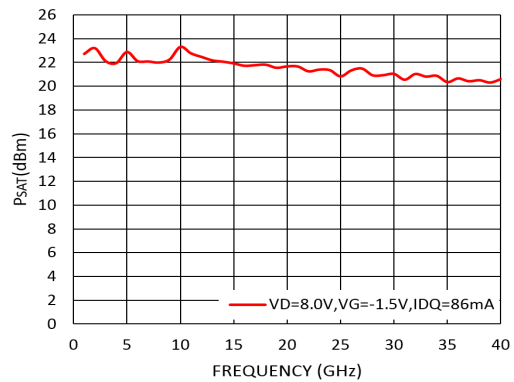
Measurement Plots: S-parameters

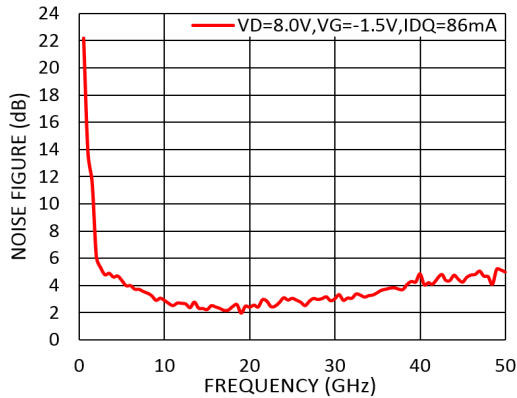


Measurement Plots: P1dB



Measurement Plots: PSAT



Measurement Plots: Noise Figure

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+8.5V
Gate Bias Voltages(VG)	-2V to 0V
RF Input Power (RFIN)@(+8V)	+10dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 8.6mW/°C above 85 °C)	0.77W
Thermal Resistance (channel to die bottom)	27°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

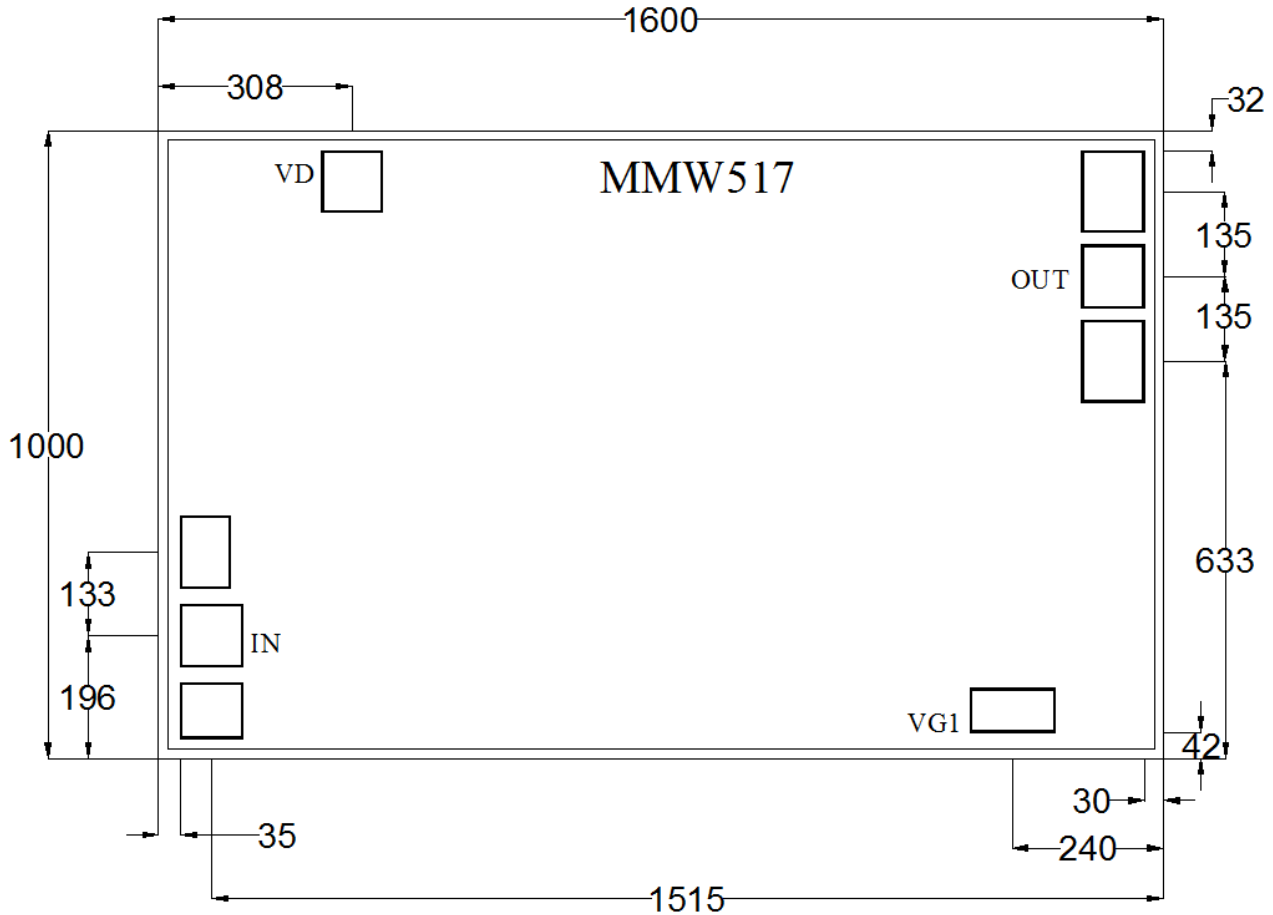
VD (V)	VG(V)	IDD (mA)
8	-1.5	86



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing:
All Dimensions in μm

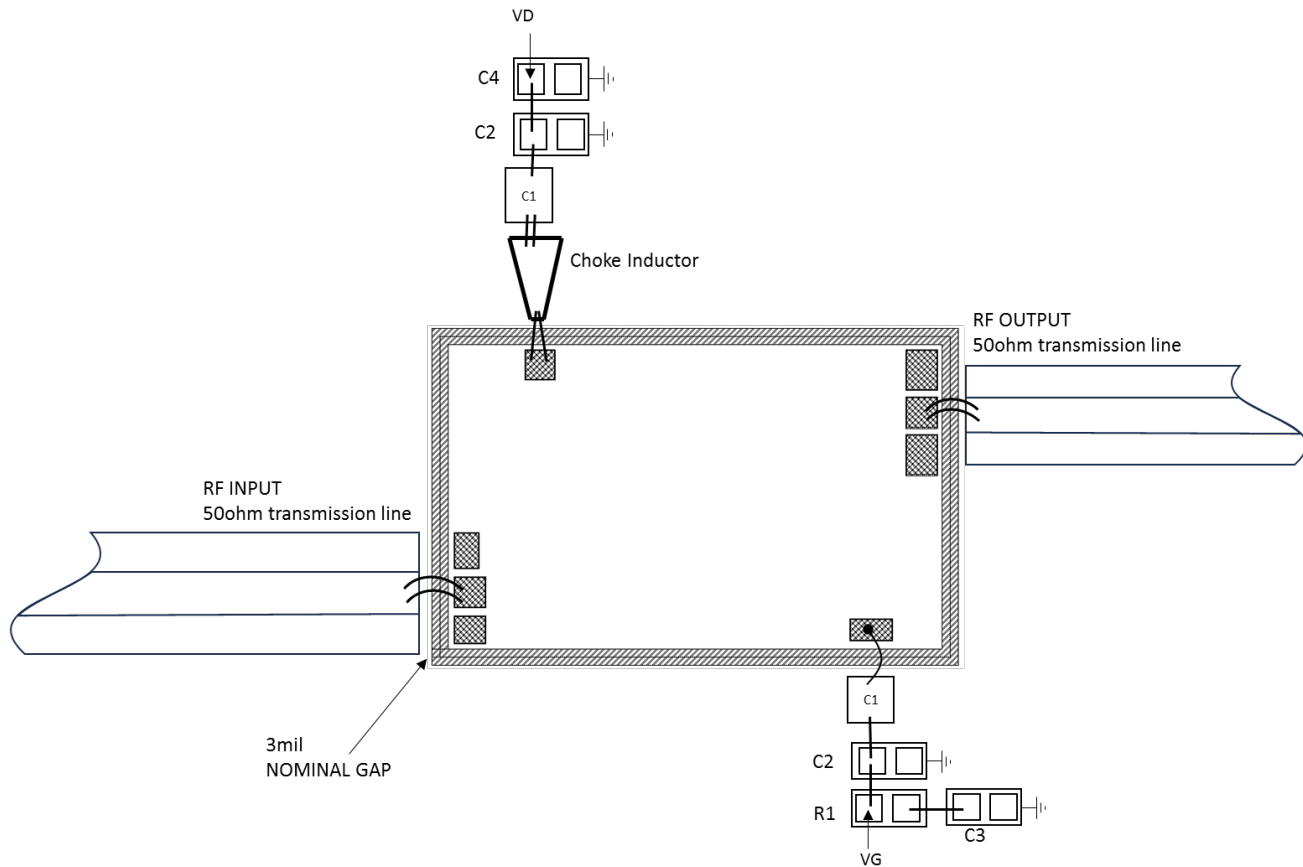


Notes:

1. Die thickness: 50 μm
2. VD bond pad is 92*92 μm^2
3. VG bond pad is 130*65 μm^2
4. RF IN/OUT bond pad is 95*95 μm^2
5. Bond pad metalization: Gold
6. Backside metalization: Gold

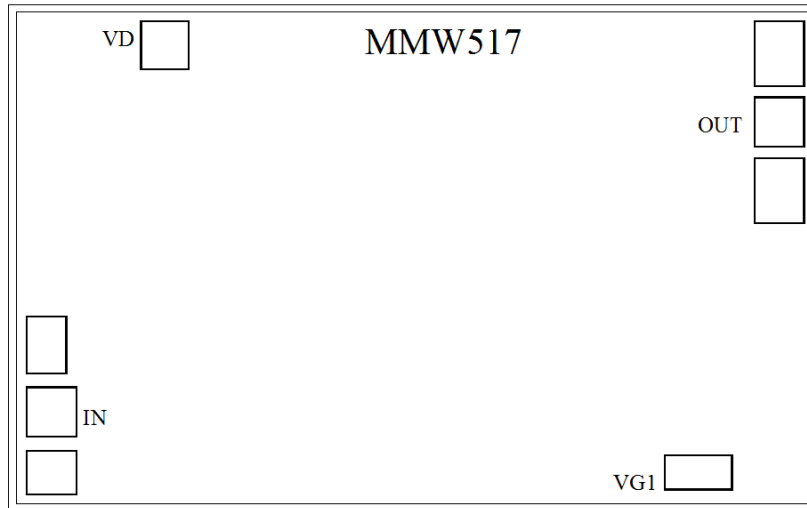


Assembly Drawing



Item	Description	Item	Description
C1	100pF Example: Presidio Part: MVB3030X103M2H5C1	C4	4.7μF Example: TDK Part: C1608X5R1A475K080AC (0603)
C2	0.01μF Example: TDK Part: C1005X7R1H103K050BB (0402)	Choke Inductor	0.425μH Example: Piconics Part: CC21T36K240G5
C3	0.1μF Example: Murata Electronics Part: GRM033Z71C104KE14D (0201)	R1	10Ω Example: Yageo Part: RC0201FR-0710RP

No	Function	Description
1	RF IN	RF signal input terminal; no blocking capacitor required.
2	RF OUT	RF signal output terminal; no blocking capacitor required.
3	VD	Drain Biases for the Amplifier.
4	VG	Gate Biases for the Amplifier.
5	Die Bottom	Die bottom must be connected to RF and dc ground.



Biassing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VG1 to -2V.
3. Set the drain bias voltages VD to +8V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 86mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1 to -2V to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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