

Features

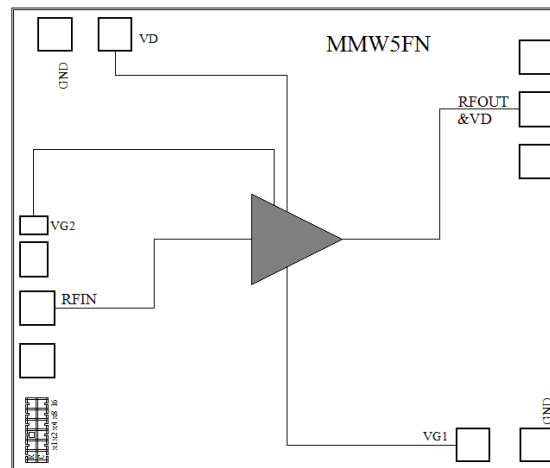
- Frequency: DC-67GHz
- Small Signal Gain: 13.5dB Typical
- Gain Flatness: ± 1.0 dB Typical
- Noise Figure: 2.5dB Typical
- P1dB: 16dBm Typical
- Psat: 19dBm Typical
- Supply Voltage:
VD = +4.5V, VG1 = -1.7V
- Input/Output: 50 Ω
- Die Size: 1.58 x 1.33 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

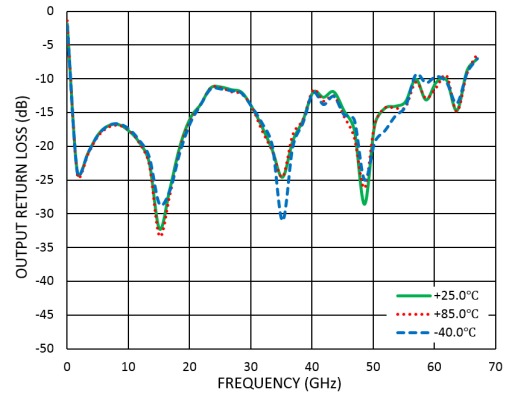
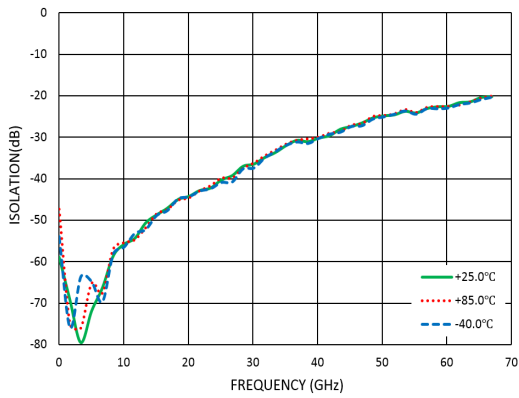
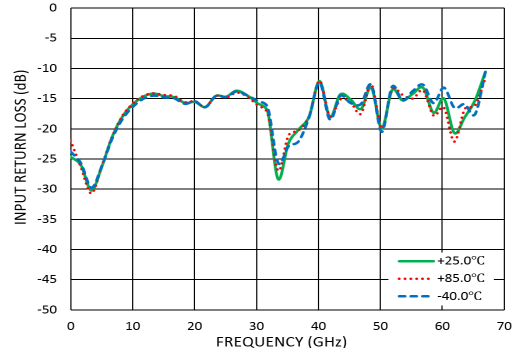
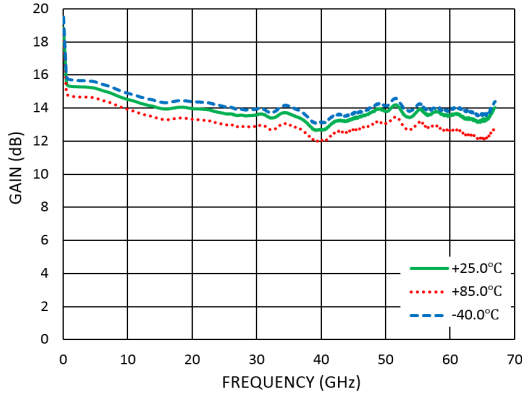
Electrical Specifications
TA = +25°C, VD = +4.5V, VG1 = -1.7V IDD = 80mA Typical

Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	DC		20	20		40	40		67	GHz
Small Signal Gain	13	14.5		12	13.5		12	13.5		dB
Gain Flatness		± 1.0			± 0.5			± 0.5		dB
Noise Figure		2.5			3.0			4.5		dB
P1dB - Output 1dB Compression	14.5	16		13.5	15		7	12		dBm
Psat - Saturated Output Power		19			17			14		dBm
OIP3 - Output Third Order Intercept		26			25			22		dBm
Input Return Loss		-15			-15			-13		dB
Output Return Loss		-16			-12			-10		dB

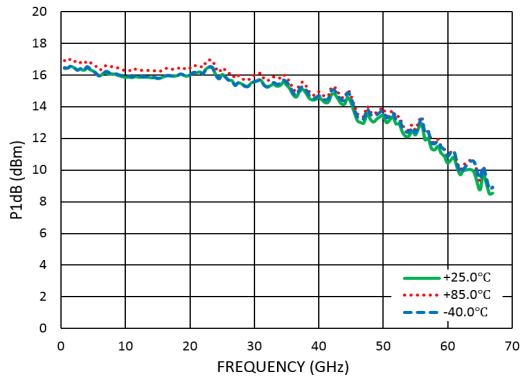
Functional Block Diagram




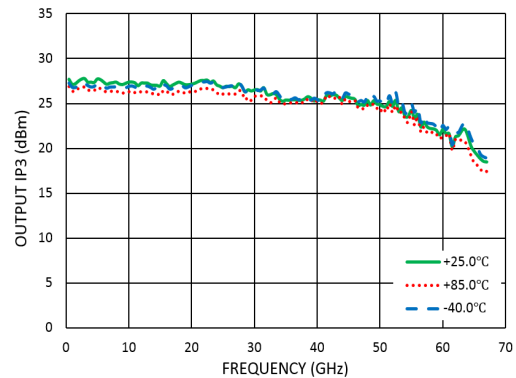
Measurement Plots: S-parameters

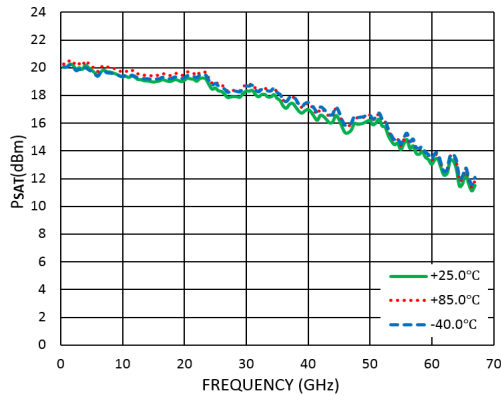
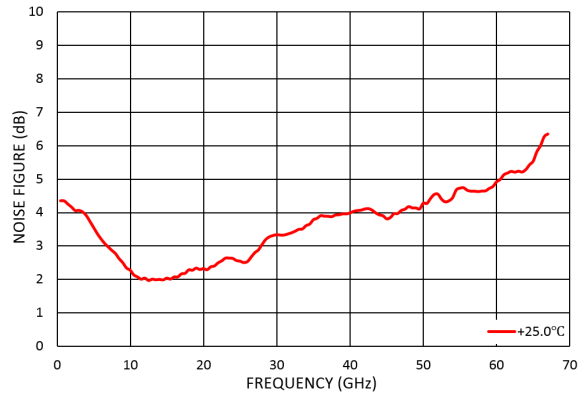


Measurement Plots: P1dB



Measurement Plots: OIP3



Measurement Plots: PsAT

Measurement Plots: Noise Figure

Absolute Maximum Ratings

Drain Bias Voltage (VD)	+7V
Gate Bias Voltages(VG)	-4V to 0.5V
RF Input Power (RFIN)@(+4.5V)	+20dBm
Channel Temperature	175 °C
Continuous P _{diss} (T = 85 °C) (derate 7.8mW/°C above 85 °C)	0.7W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

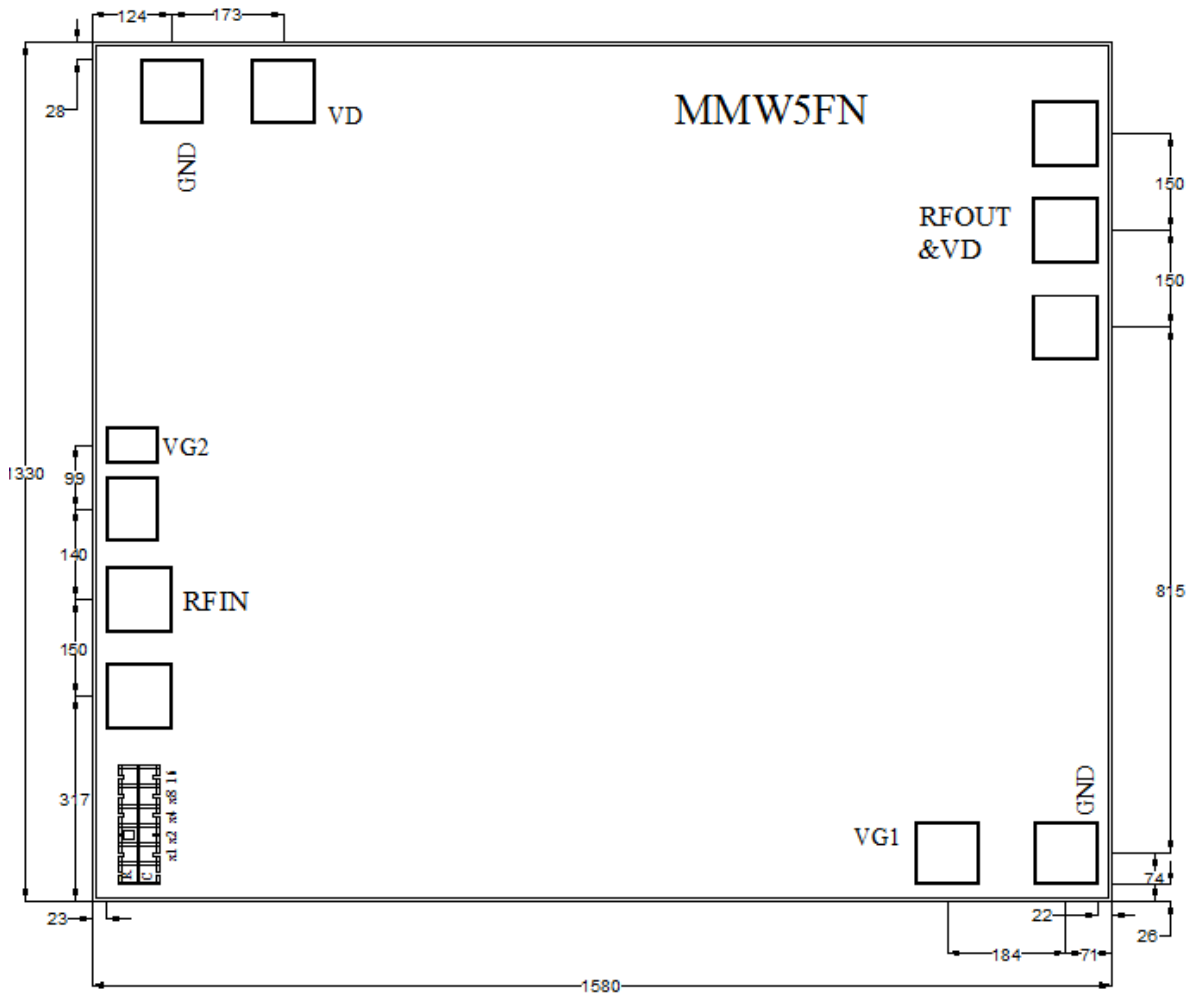
Typical Supply Current vs. VD, VG

VD (V)	VG1 (V)	VG2 (V)	IDD (mA)
4.5	-1.7	NA	80


**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**



Outline Drawing: All Dimensions in μm

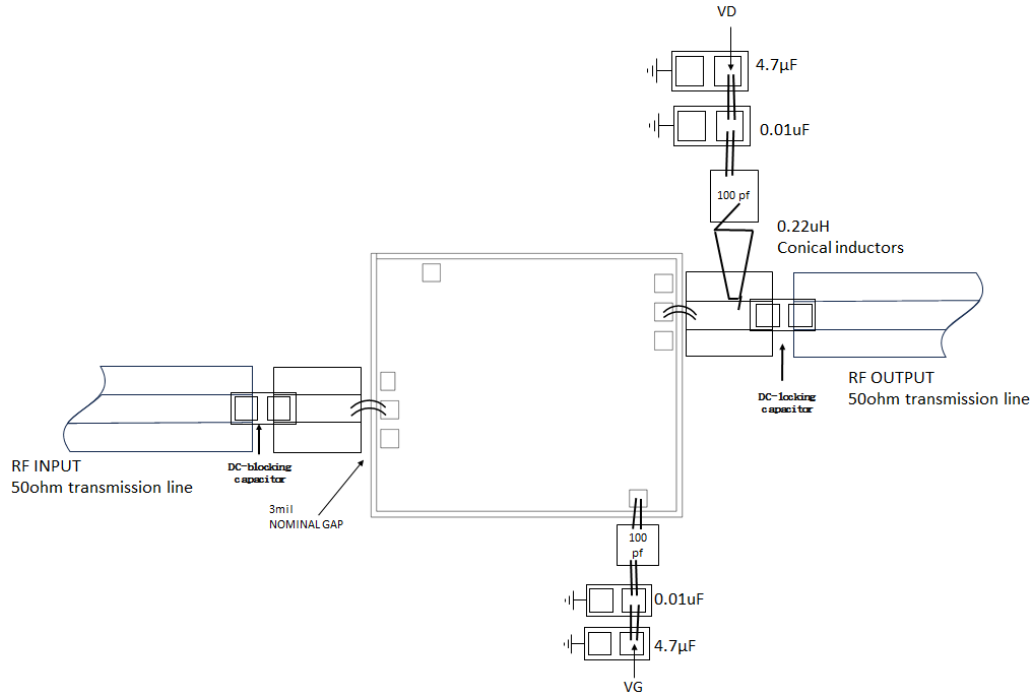


Notes:

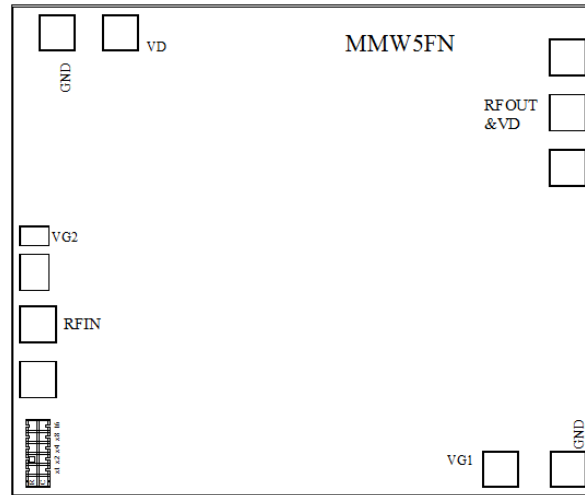
1. Die thickness: 100 μm
2. DC bond pad is 100*100 μm^2
3. RF IN/OUT bond pad is 100*100 μm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold



Assembly Drawing



No.	Mnemonic	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VD	Drain Biases for the Amplifier. External bypass capacitors of 4.7µf and 0.01 µf and 100 pf are required for these pads.
4	VG1	Amplifier Gate Controls. External bypass capacitors of 4.7µf and 0.01 µf and 100 pf are required for these pads. ESD protection diodes are included and turn on below -4V.
5	VG2	NA
6	Die Bottom	Die bottom must be connected to RF and dc ground.



Biassing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages, VG1 to -4V.
3. Set the drain bias voltages VD to +4.5V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 80mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1 to -4V to achieve a $I_{DQ} = 0$ mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.

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