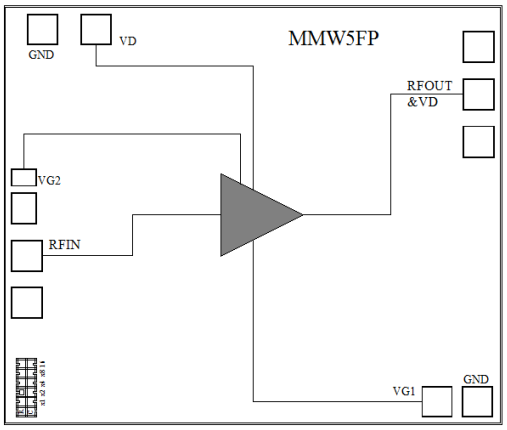
Features

- Frequency: DC-67GHz
- Small Signal Gain: 13.5dB Typical
- Gain Flatness: ±1.5dB Typical
- Noise Figure: 3.5dB Typical
- P1dB: 18dBm Typical
- Psat: 21.5dBm Typical
- Supply Voltage:
  VD =+8V,VG1=-0.9V
- Input/Output: 50Ω
- Die Size: 1.58 x 1.33 x 0.1mm

Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Functional Block Diagram

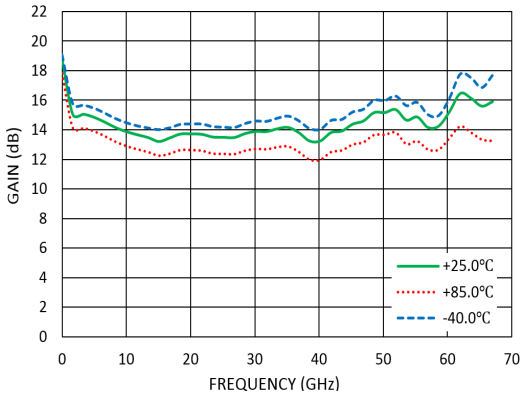


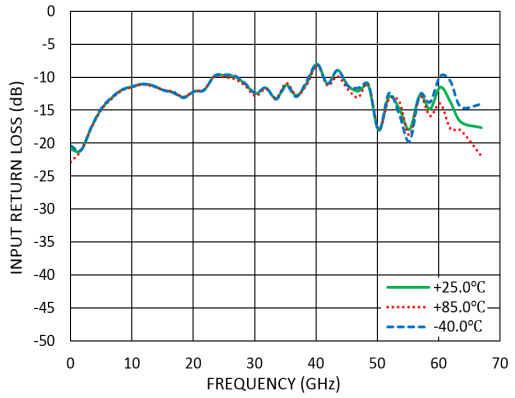
Electrical Specifications

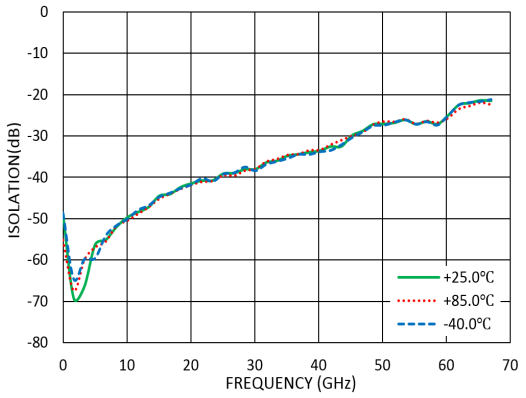
TA = +25°C, VD=+8V,VG1= -0.9V IDD = 140mA Typical

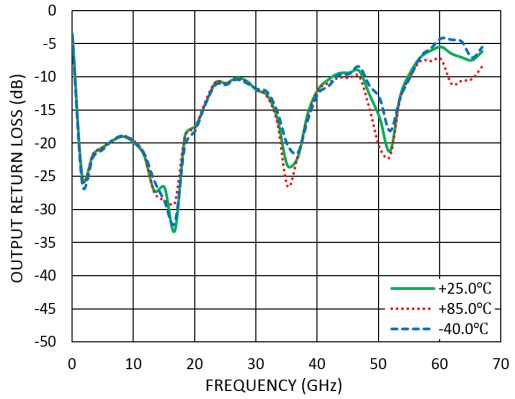
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	DC		20	20		40	40		67	GHz
Small Signal Gain	12.5	13.5		12	13		12	14.5		dB
Gain Flatness		±1.0			±0.5			±1.5		dB
Noise Figure		3.5			4.0			6.0		dB
P1dB - Output 1dB Compression	16	18		15	17		12	14		dBm
Psat - Saturated Output Power		21.5			20.5			17		dBm
OIP3 - Output Third Order Intercept		26.5			26.5			23		dBm
Input Return Loss		-12			-10			-10		dB
Output Return Loss		-18			-10			-7		dB

Measurement Plots: S-parameters

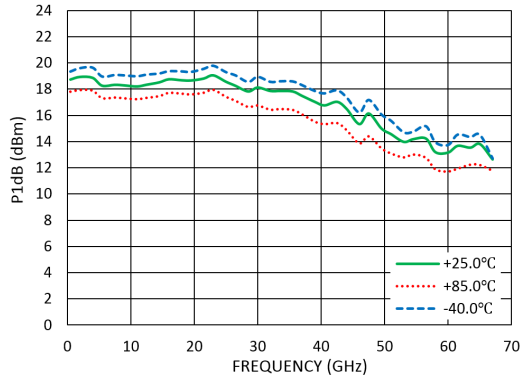




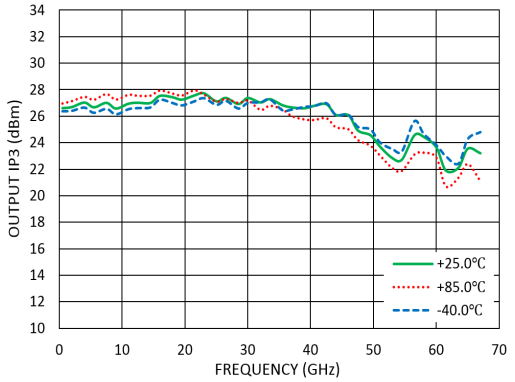




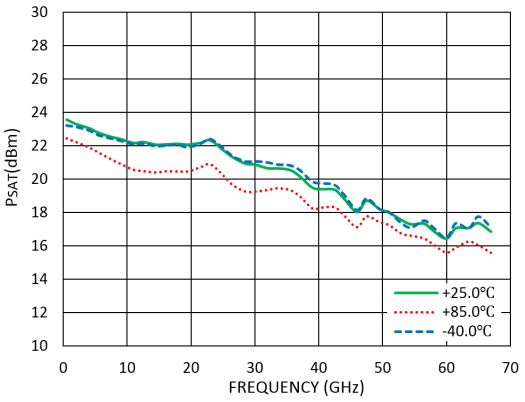
Measurement Plots: P1dB



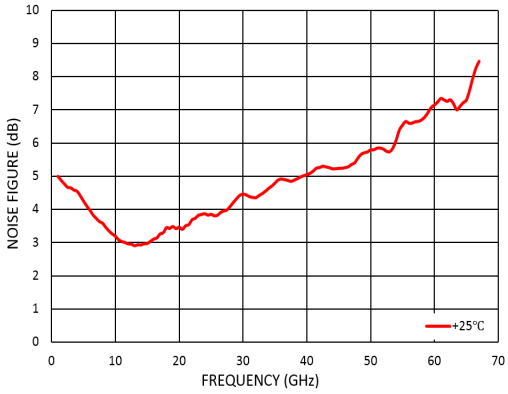
Measurement Plots: OIP3



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

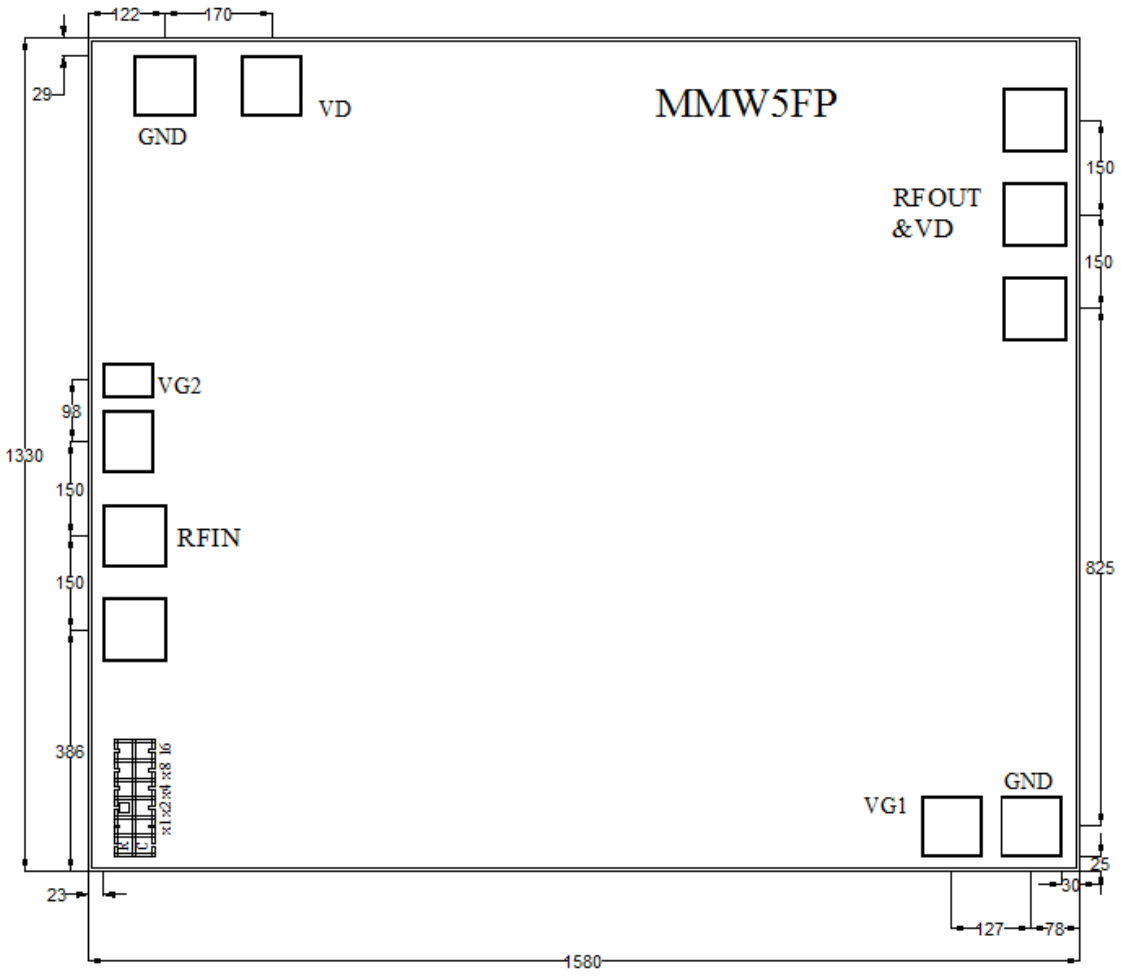
Drain Bias Voltage (VD)	+8.5V
Gate Bias Voltages(VG)	–4V to 0.5V
RF Input Power (RFIN)@(+8V)	+23dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 13.3mW/°C above 85 °C)	1.2W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

Typical Supply Current vs. VD,VG

VD (V)	VG1 (V)	VG2 (V)	IDD (mA)
8	-0.9	NA	140

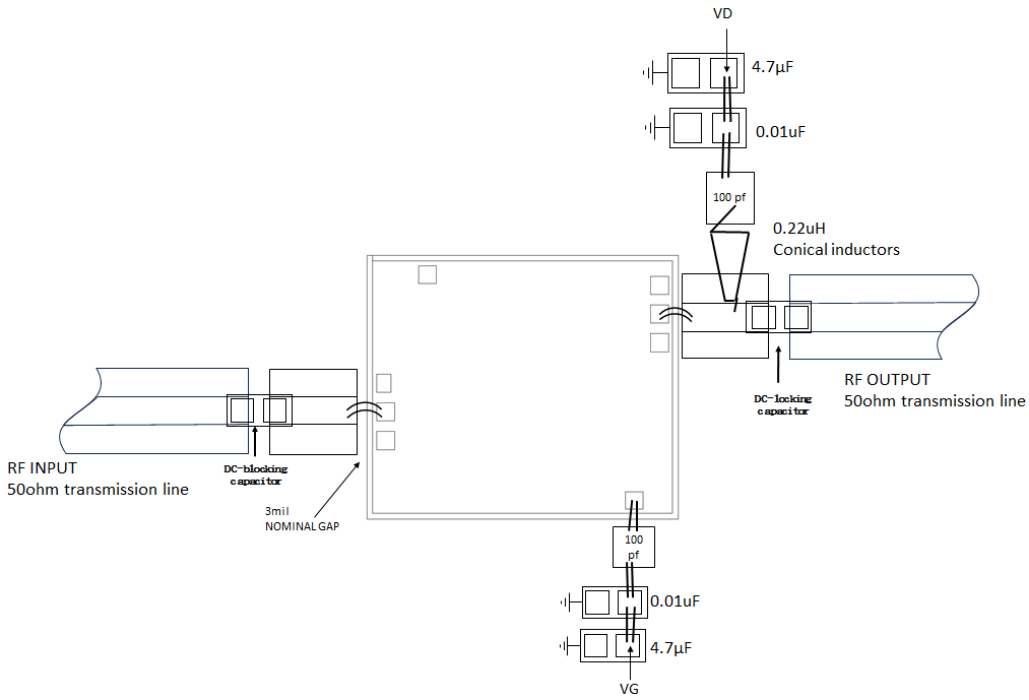
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:
All Dimensions in µm

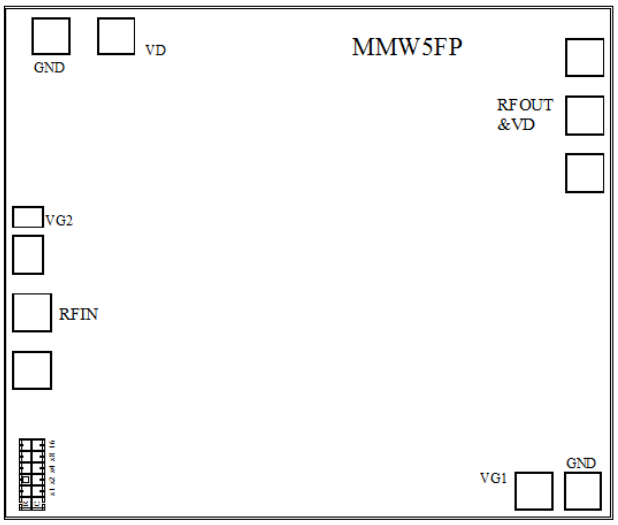


Notes:
1. Die thickness: 100µm
2. DC bond pad is 100*100µm^2
3. RF IN/OUT bond pad is 100*100µm^2
4. Bond pad metalization: Gold
5. Backside metalization: Gold

Assembly Drawing



No.	Mnemonic	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VD	Drain Biases for the Amplifier. External bypass capacitors of 4.7µf and 0.01 µf and 100 pf are required for these pads.
4	VG1	Amplifier Gate Controls. External bypass capacitors of 4.7µf and 0.01 µf and 100 pf are required for these pads. ESD protection diodes are included and turn on below −4V.
5	VG2	NA
6	Die Bottom	Die bottom must be connected to RF and dc ground.



Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltages,VG1 to −4V.
3. Set the drain bias voltages VD to +8V .
4. Increase the gate bias voltages to achieve a quiescent supply current of 140mA.
5. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, VG1 to −4V to achieve a I_{DQ} = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the all gate bias voltages to 0 V.