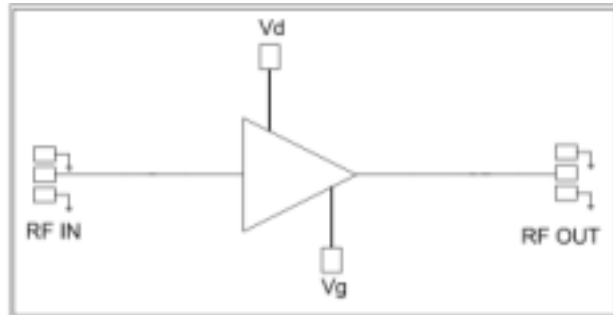


**Features**

- Frequency: DC-20GHz
- Small Signal Gain: 13dB
- Gain Flatness:  $\leq \pm 1.6\text{dB}@DC-20\text{GHz}$
- Noise Figure:  $\leq 4\text{dB}$
- P1dB: 18dBm
- Psat: 21dBm
- Power Supply: +5V/80mA
- Input/Output: 50Ω
- Die Size: 2.94 x 1.35 x 0.1 mm

**Typical Applications**

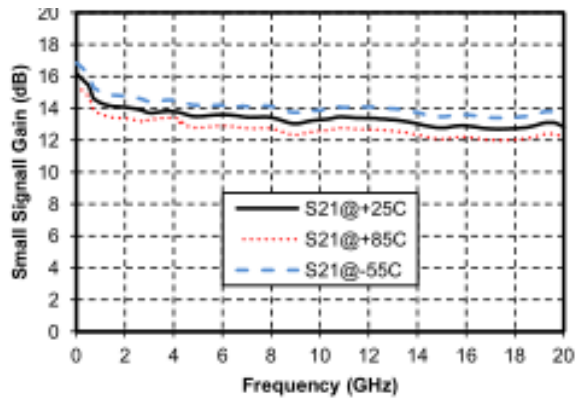
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

**Functional Block Diagram**

**Electrical Specifications**
**TA = +25°C, Vd = +5V, \*Ids=80mA**

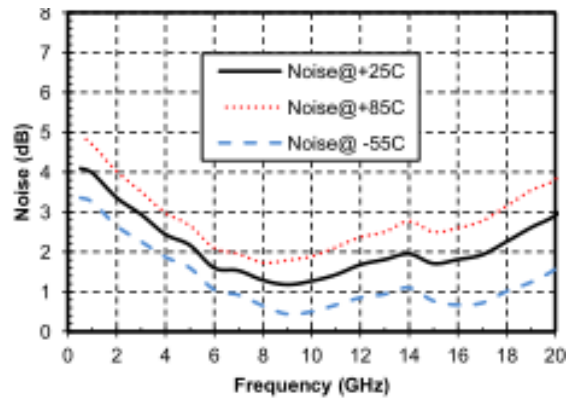
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
<b>Frequency</b>	<b>DC-6</b>			<b>6-12</b>			<b>12-20</b>			<b>GHz</b>
<b>Small Signal Gain</b>	<b>13.5</b>	<b>14</b>	<b>16</b>	<b>13.3</b>	<b>13.5</b>	<b>13.6</b>	<b>12.8</b>	<b>13</b>	<b>13.3</b>	<b>dB</b>
<b>Gain Flatness</b>		<b>±1.75</b>			<b>±0.15</b>			<b>±0.25</b>		<b>dB</b>
<b>Noise Figure</b>	<b>1.8</b>	<b>3.4</b>	<b>4.2</b>	<b>1.4</b>	<b>1.7</b>	<b>1.9</b>	<b>1.7</b>	<b>2.1</b>	<b>3.0</b>	<b>dB</b>
<b>Output 1dB Compression (P1dB)</b>	<b>18</b>	<b>18.5</b>	<b>18.5</b>	<b>17.7</b>	<b>18</b>	<b>18.5</b>	<b>17</b>	<b>18</b>	<b>18.7</b>	<b>dBm</b>
<b>Saturated Output Power (Psat)</b>	<b>20.5</b>	<b>21</b>	<b>21.5</b>	<b>21</b>	<b>21.5</b>	<b>21.8</b>	<b>19.5</b>	<b>21</b>	<b>22</b>	<b>dBm</b>
<b>Input Return Loss</b>		<b>20</b>			<b>18</b>			<b>12</b>		<b>dB</b>
<b>Output Return Loss</b>		<b>20</b>			<b>30</b>			<b>13</b>		<b>dB</b>

**\* Adjust VG (-2V-0V) to obtain device current of 80mA. (approximately -0.95V)**

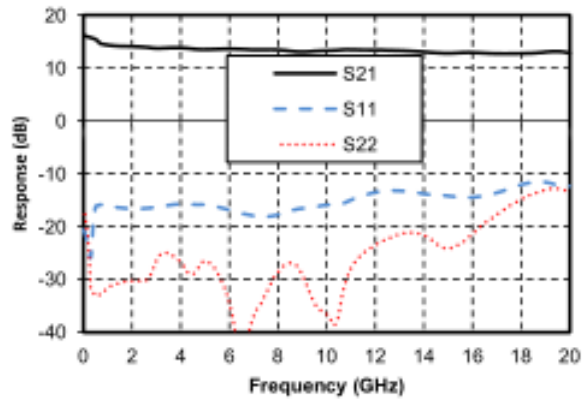
Gain vs. Frequency



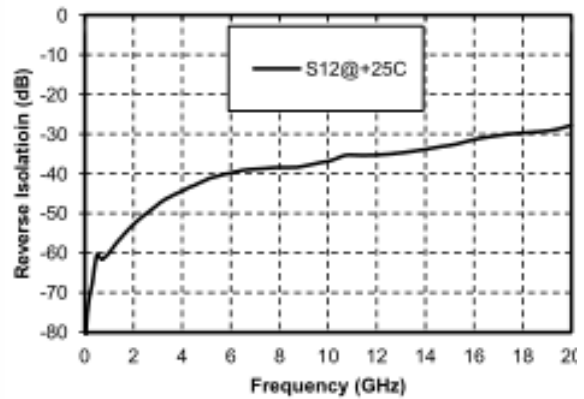
Noise Figure vs. Frequency



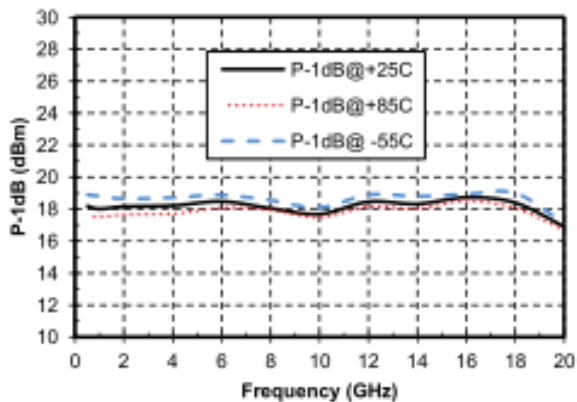
Gain & Return Loss vs. Frequency



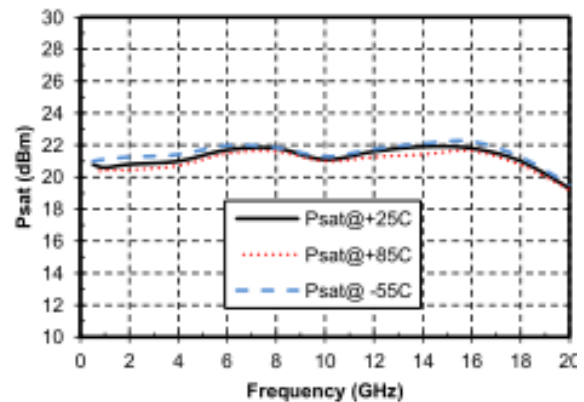
Reverse Isolation vs. Frequency



P1dB vs. Frequency

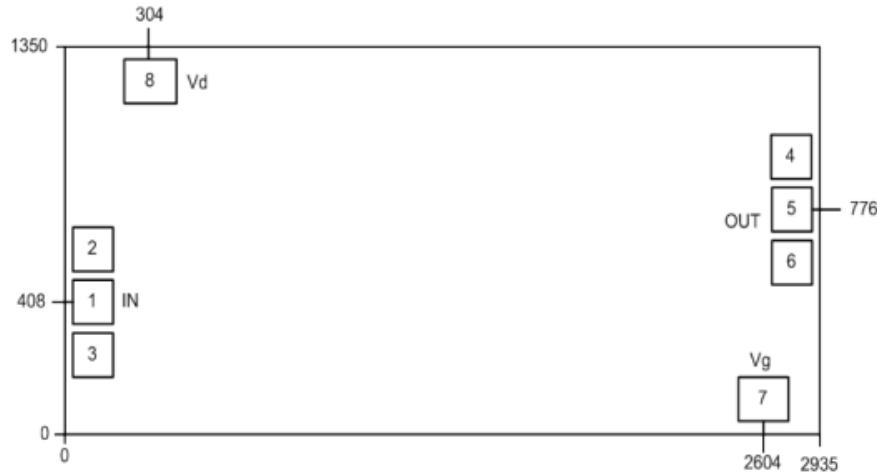


Psat vs. Frequency





**Outline Drawing:**  
All Dimensions in  $\mu\text{m}$

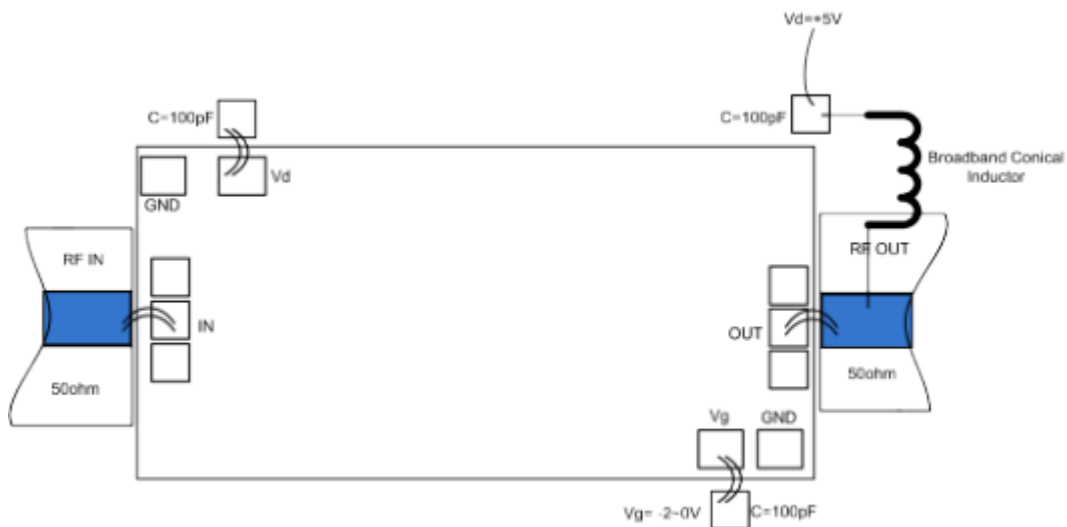


**Pad Description**

Pad	Function	Description	Equivalent Circuit
1	RF IN	Signal input terminal, connected to 50 $\Omega$ circuit; blocking capacitor required.	
5	RF OUT	Signal output terminal, connected to 50 $\Omega$ circuit; blocking capacitor required; external DC biasing network required; drain current provided. Refer to following assembly drawing or contact manufacturer.	
7	Vg	Amplifier gate bias; connect to 100pF bypass capacitor.	
8	Vd	Amplifier drain bias, connect to external 100pF bypass capacitor.	
2, 3, 4, 6, die bottom	GND	Die bottom must be connected to RF/DC ground.	



## Assembly Drawing



### Notes:

1. Die thickness: 100um
2. Typical bond pad is 100\*100  $\mu\text{m}^2$
3. Bond pad metalization: Gold
4. Backside metalization: Gold
5. Backside of the die (GND)
6. No connection required for unlabeled bond pads

### Maximum Ratings:

1. Maximum drain voltage: +14V
2. Maximum gate bias: -3V
3. Maximum input power: +20dBm
4. Operating temperature: -55°C to +85°C
5. Storage temperature: -65°C to +150°C