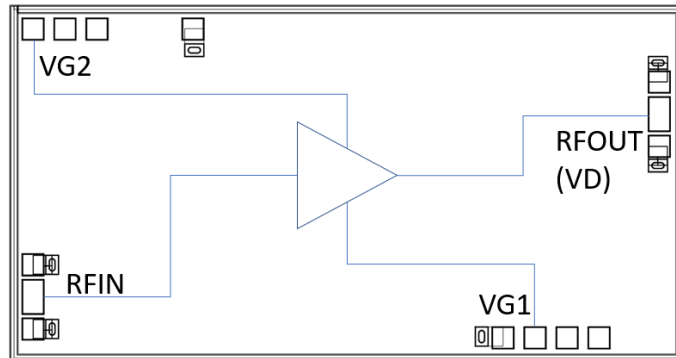


**Features**

- Frequency: DC-20GHz
- Small Signal Gain: 18.5dB
- Gain Flatness:  $\leq \pm 1.8$  dB@ DC-20GHz
- Noise Figure:  $\leq 4$ dB
- P1dB = 22.5 dBm
- Psat = 24.5 dBm
- Power Supply: +8V/145mA
- Input/Output: 50 $\Omega$
- Die Size: 3.12 x 1.63 x 0.1 mm

**Typical Applications**

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

**Functional Block Diagram**

**Electrical Specifications**

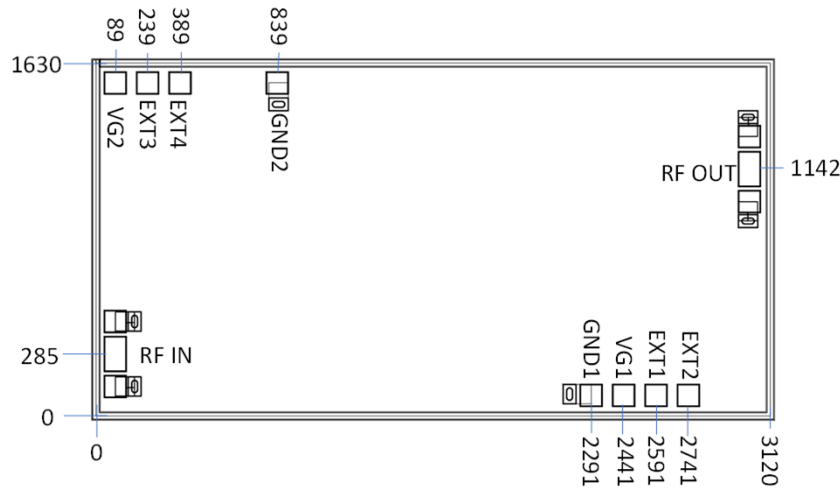
TA = +25°C, VD = +8V, VG1 = -0.4V, VG2 = 3.6V, ID = 145mA

Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
<b>Frequency</b>	<b>DC-6</b>			<b>6-12</b>			<b>12-20</b>			<b>GHz</b>
<b>Small Signal Gain</b>	18.4	18.9	21.2	17.5	18.2	18.4	16.2	17.1	17.6	<b>dB</b>
<b>Gain Flatness</b>		$\pm 0.9$			$\pm 0.5$			$\pm 0.7$		<b>dB</b>
<b>Noise Figure</b>	2.2	4	9.7	2.0	2.1	2.3	2.3	2.6	3.2	<b>dB</b>
<b>Output 1dB Compression (P1dB)</b>	22.4	22.5	22.8	22.4	22.5	22.7	21.8	22.9	23	<b>dBm</b>
<b>Saturated Output Power (Psat)</b>		24.5			24.5			24.9		<b>dBm</b>
<b>Input Return Loss</b>		18			20			21		<b>dB</b>
<b>Output Return Loss</b>		27			19			13		<b>dB</b>

\* Adjust VG1, VG2 slightly to obtain device current of 145mA.



**Outline Drawing:**  
All Dimensions in  $\mu\text{m}$

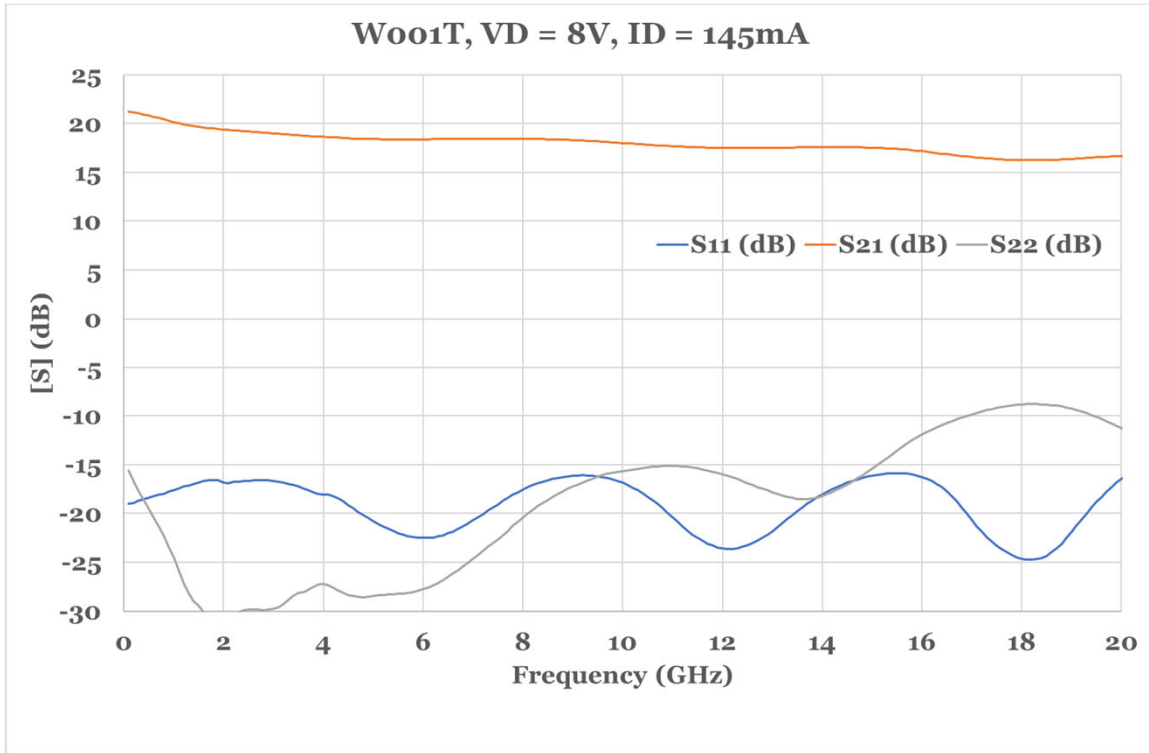


**Pad Description**

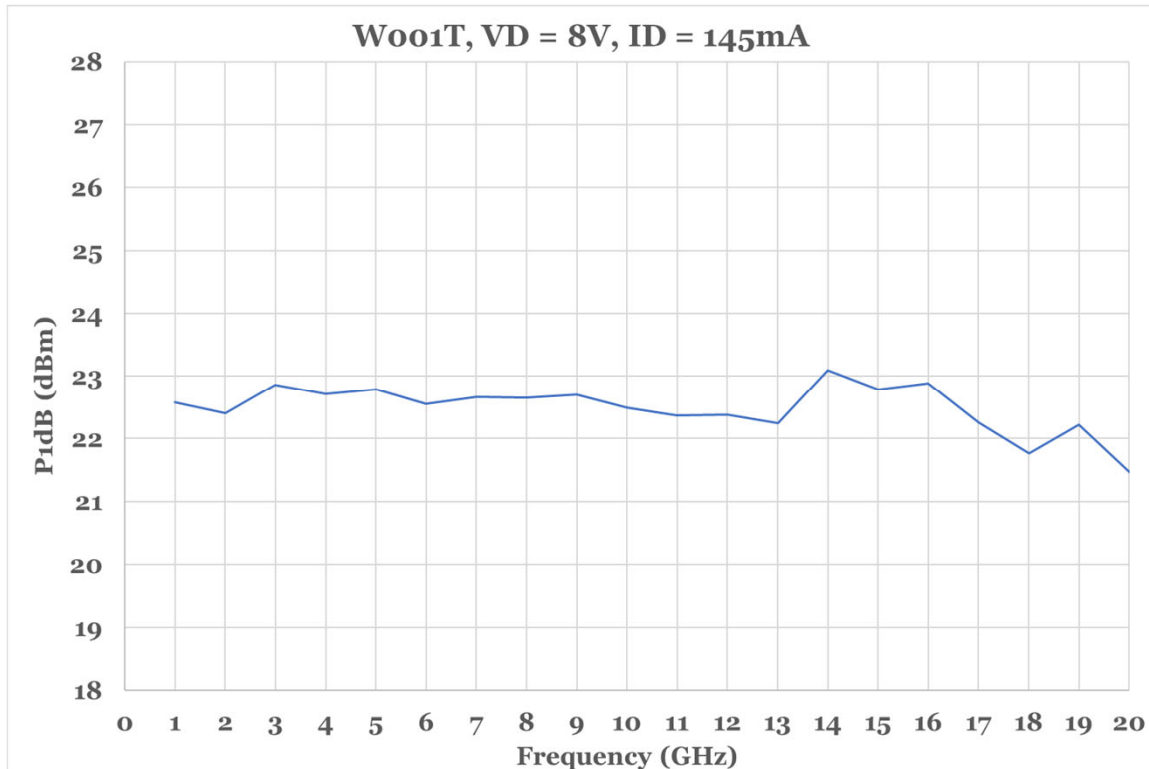
No	Function	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required; drain current provided.
3	VG1	Amplifier 1 <sup>st</sup> gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
4	VG2	Amplifier 2 <sup>nd</sup> gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
5	EXT1	External bypass pad; connect to external 0.47uF bypass capacitor.
6	EXT2	External bypass pad; connect to external 1000pF bypass capacitor.
7	EXT3	External bypass pad; connect to external 1000pF bypass capacitor.
8	EXT4	External bypass pad; connect to external 0.47uF bypass capacitor.
9	GND1	Ground pad.
10	GND2	Ground pad.



### Measurement Plots: S-parameters

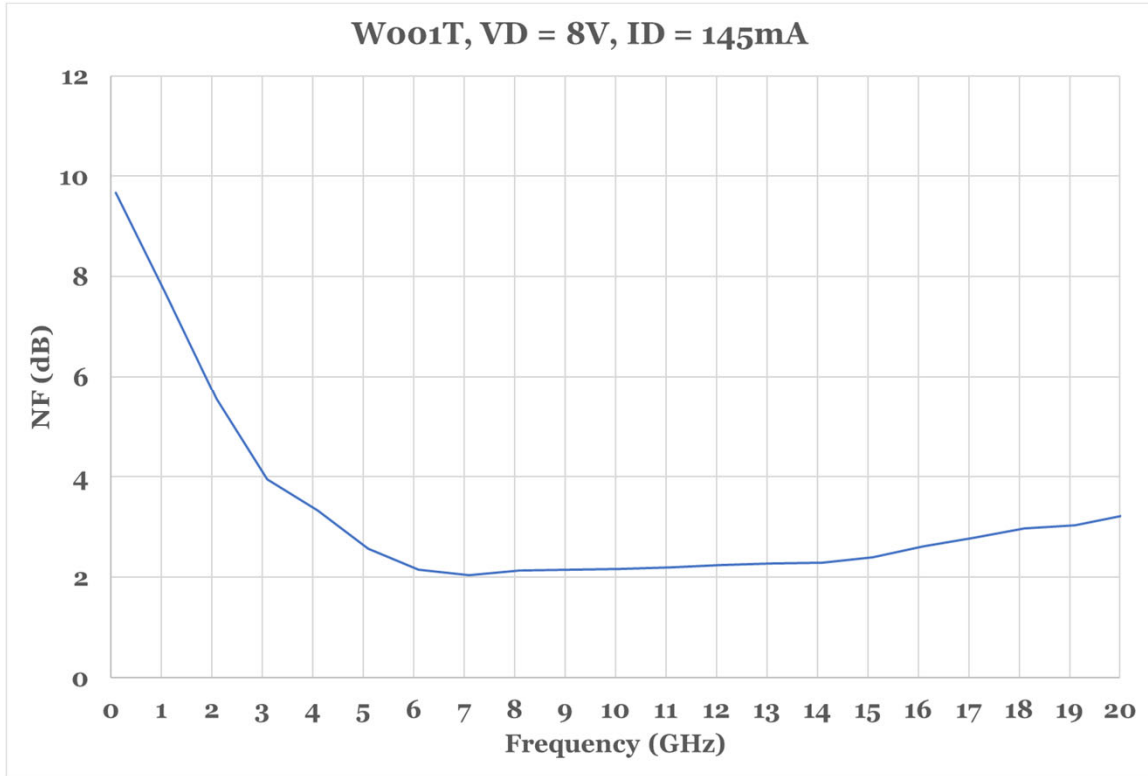


### Measurement Plots: P1dB

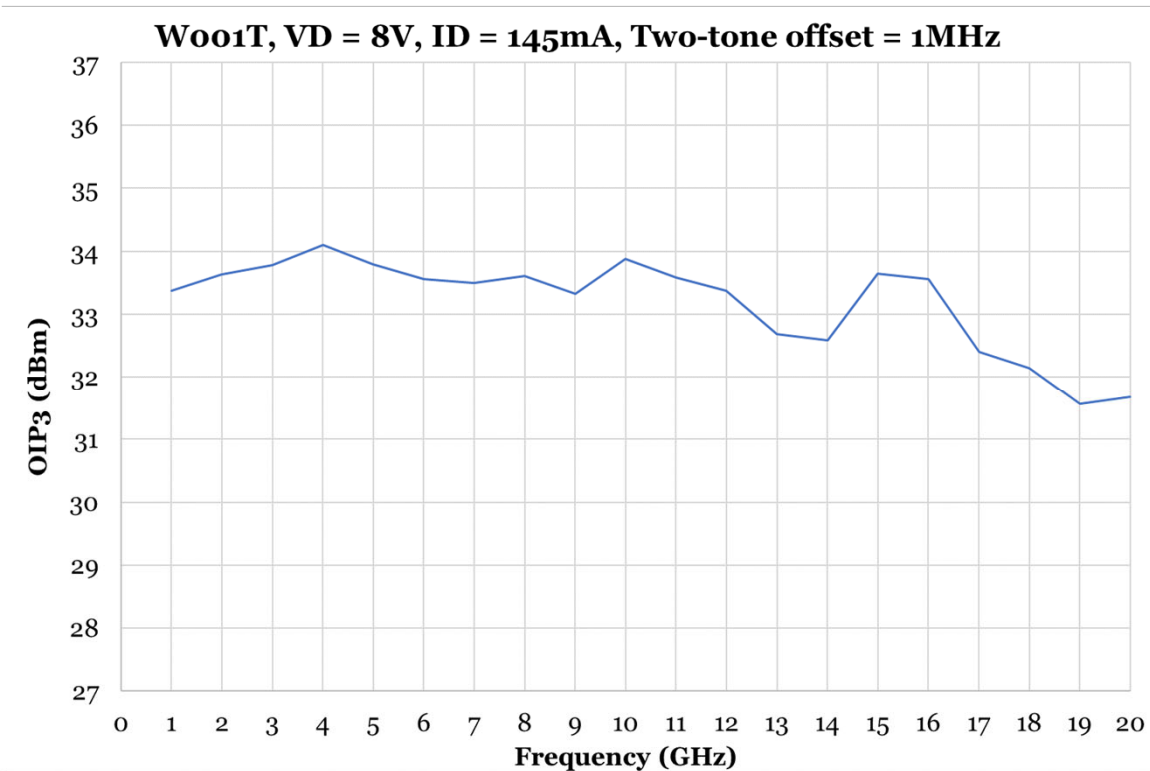




### Measurement Plots: Noise Figure

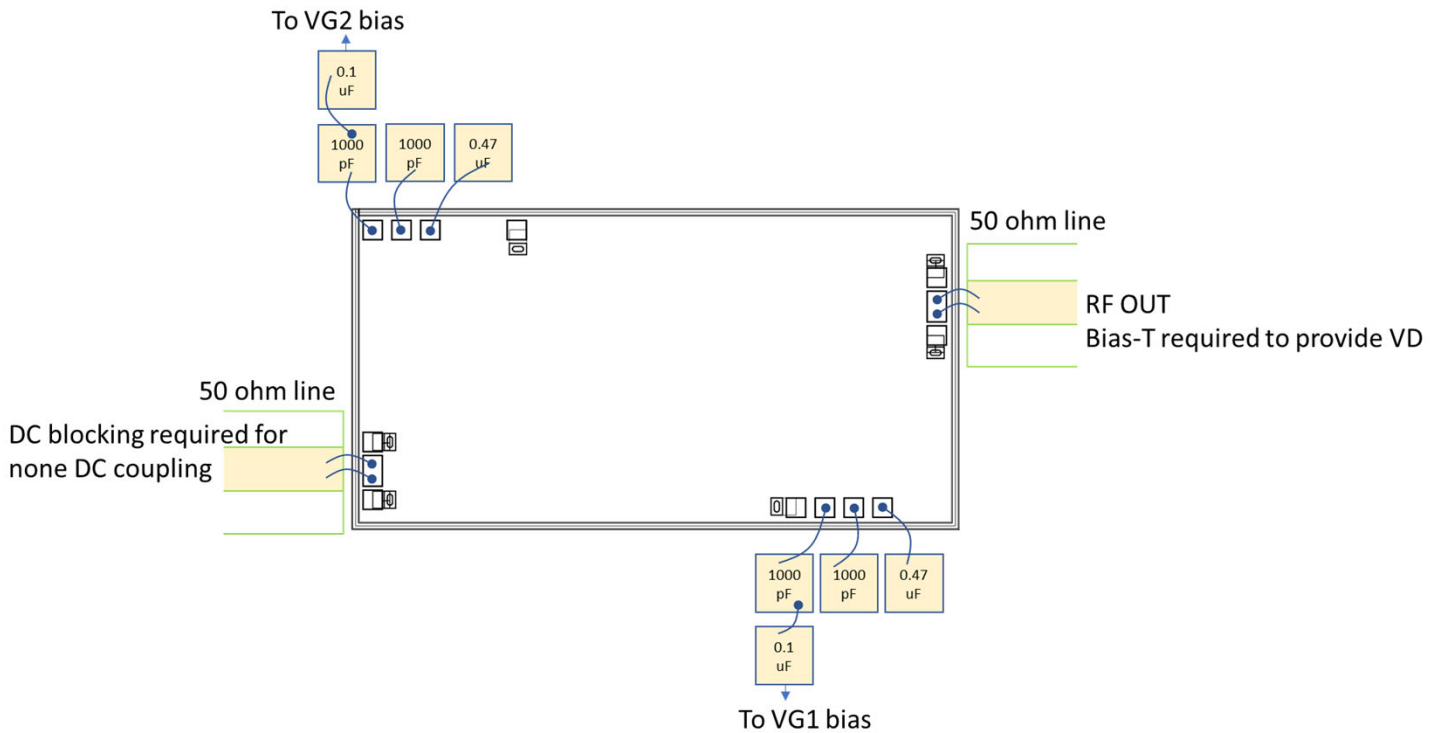


### Measurement Plots: OIP3





### Assembly Drawing



#### Notes:

1. Die thickness: 100um
2. DC bond pad is 100 x 100  $\mu\text{m}^2$
3. RF IN/OUT bond pad is 100 x 160  $\mu\text{m}^2$
4. Bond pad metalization: Gold
5. Backside metalization: Gold
6. Backside of the die (GND)

#### Maximum Ratings:

1. Maximum drain voltage: +10V
2. Maximum gate bias: -3V
3. Maximum input power: +20dBm
4. Operating temperature: -55°C to +85°C
5. Storage temperature: -65°C to +150°C