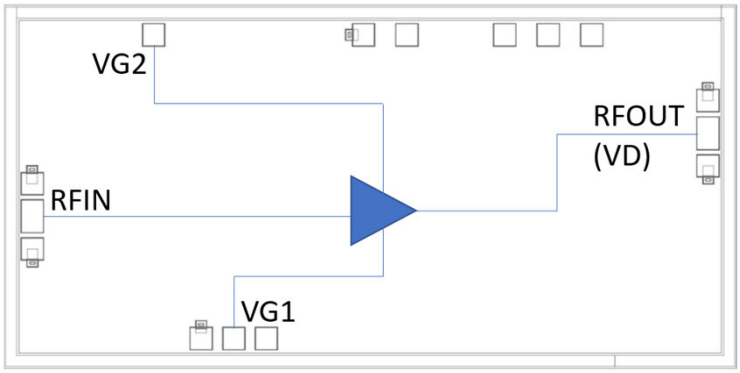
V1.0.1

GaAs MMIC
Wide-band Amplifier
DC-55GHz

Features

- Frequency: DC-55GHz
- Small Signal Gain: 15 dB
- Gain Flatness: ≤±1 dB@ 3-55GHz
- Noise Figure: 3 dB @ 30GHz
- P1dB: 21 dBm @ 30GHz
- Psat = 23.5 dBm @ 30GHz
- Power Supply: +8V/200mA
- Input/Output: 50Ω
- Die Size: 3.3 x 1.6 x 0.05 mm

Functional Block Diagram



Typical Applications

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Electrical Specifications

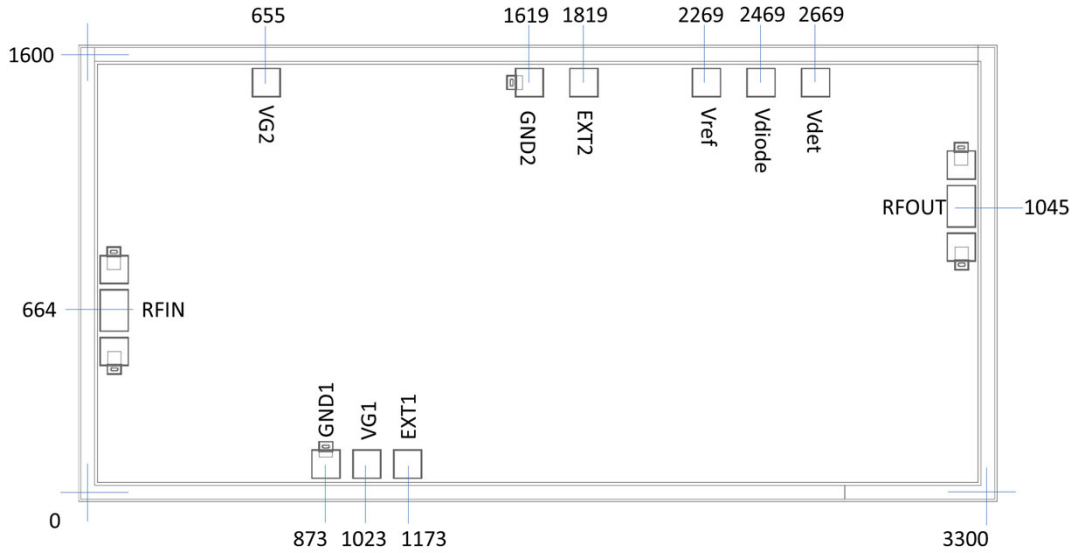
TA = +25°C, VD = +8V, VG1 = -0.4V, VG2 = 3.6V, ID = 200mA

Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	DC-4			4-44			44-55			GHz
Small Signal Gain	16	16	19	15	15.5	16	15	15	16	dB
Gain Flatness		±2			±0.5			±0.5		dB
Noise Figure	4	4	5	2.0	3	4	4	5	6	dB
Output 1dB Compression (P1dB)	> 23			> 21			> 17			dBm
Saturated Output Power (Psat)	> 25			> 23.5			> 20.5			dBm
Input Return Loss	< 10									dB
Output Return Loss	< 10									dB

* Adjust VG1, VG2 slightly to obtain device current of 200 mA.

Outline Drawing:

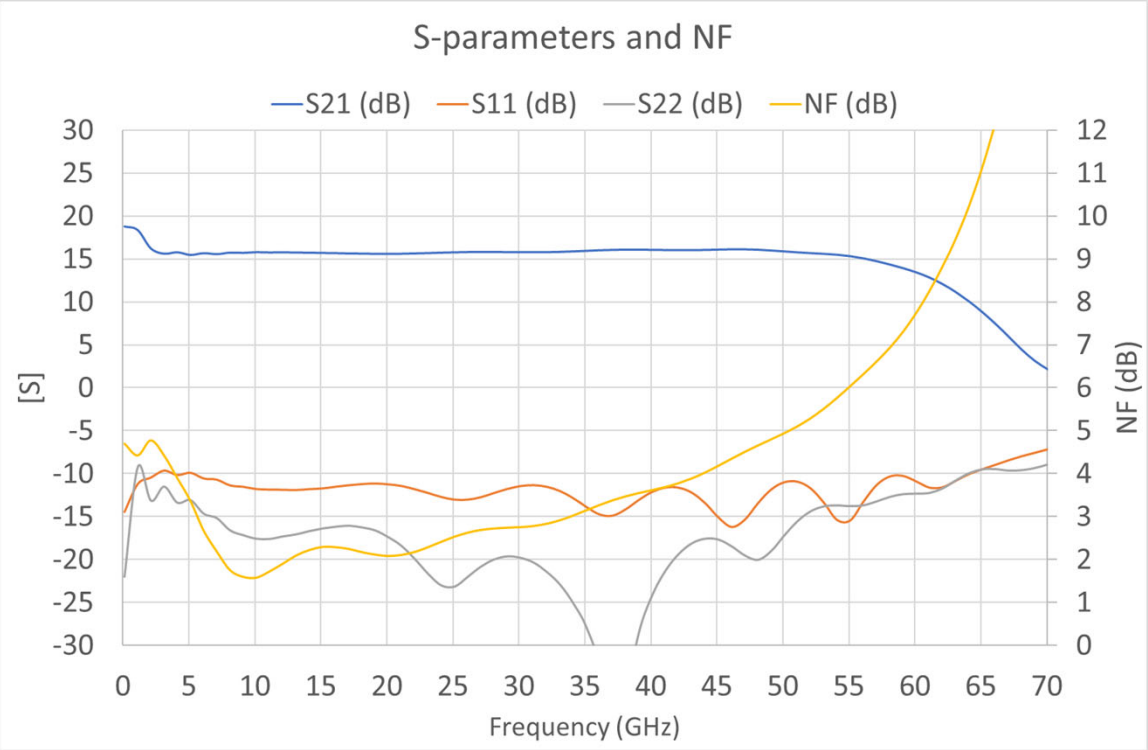
All Dimensions in μm



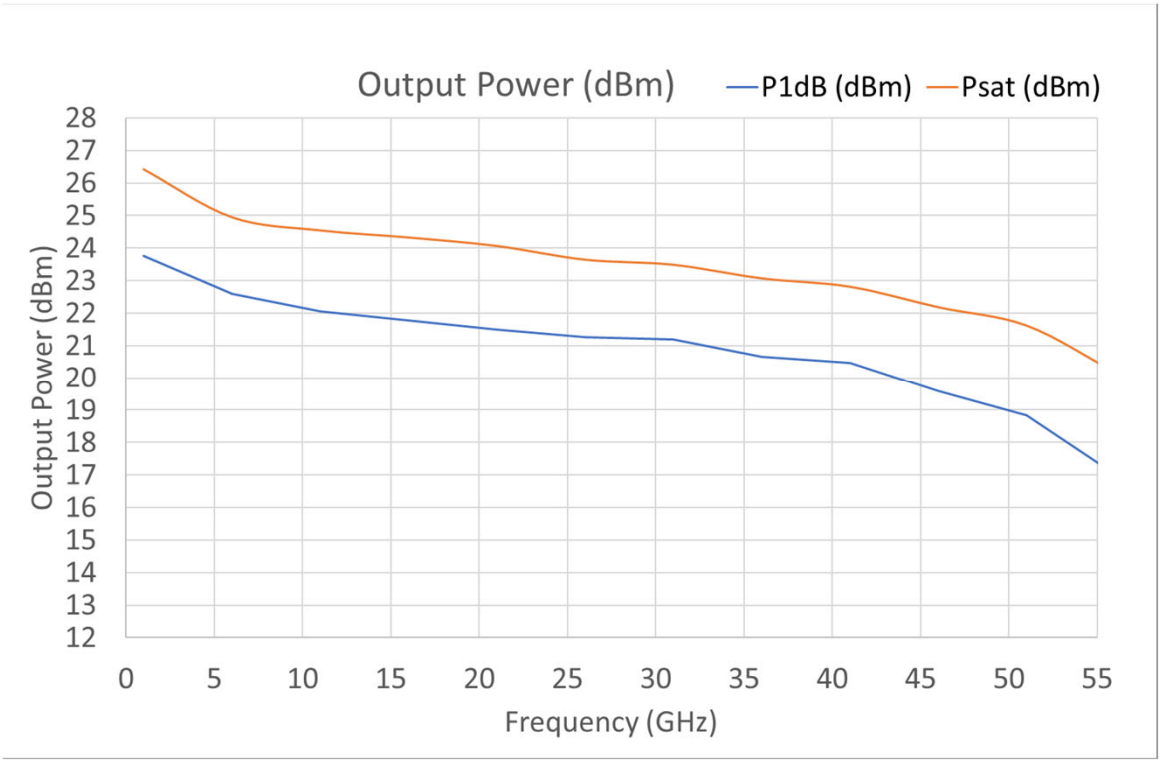
Pad Description

No	Function	Description
1	RF IN	Signal input terminal, connected to 50Ω circuit, DC-coupled
2	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required; external DC biasing network required.
3	VG1	Amplifier 1st gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
4	VG2	Amplifier 2nd gate bias; connect to external 1000pF and 0.01uF bypass capacitors.
5	EXT1	External bypass pad; connect to external bypass capacitors.
6	EXT2	External bypass pad; connect to external bypass capacitors.
7	Vdiode	Diode biasing voltage
8	Vref	Reference diode output voltage
9	Vdet	Detector output voltage
10	GND1, GND2	Ground pads.

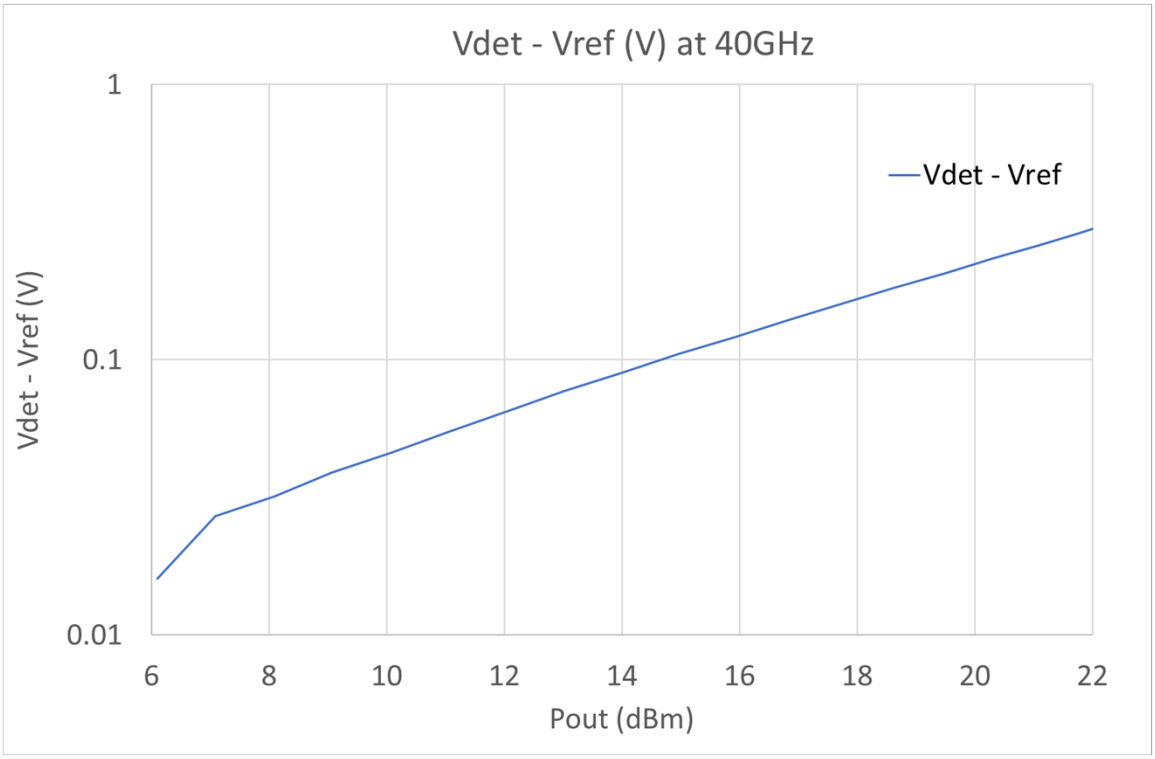
S-parameters and NF



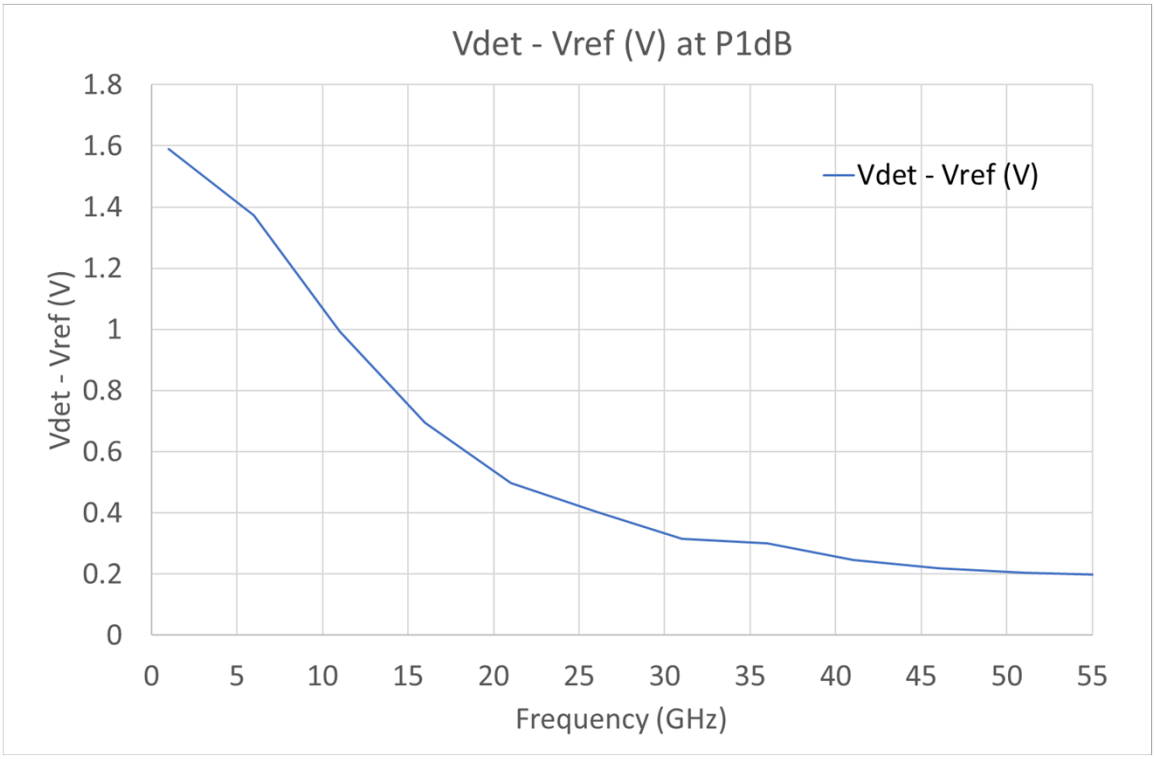
P1dB and Psat



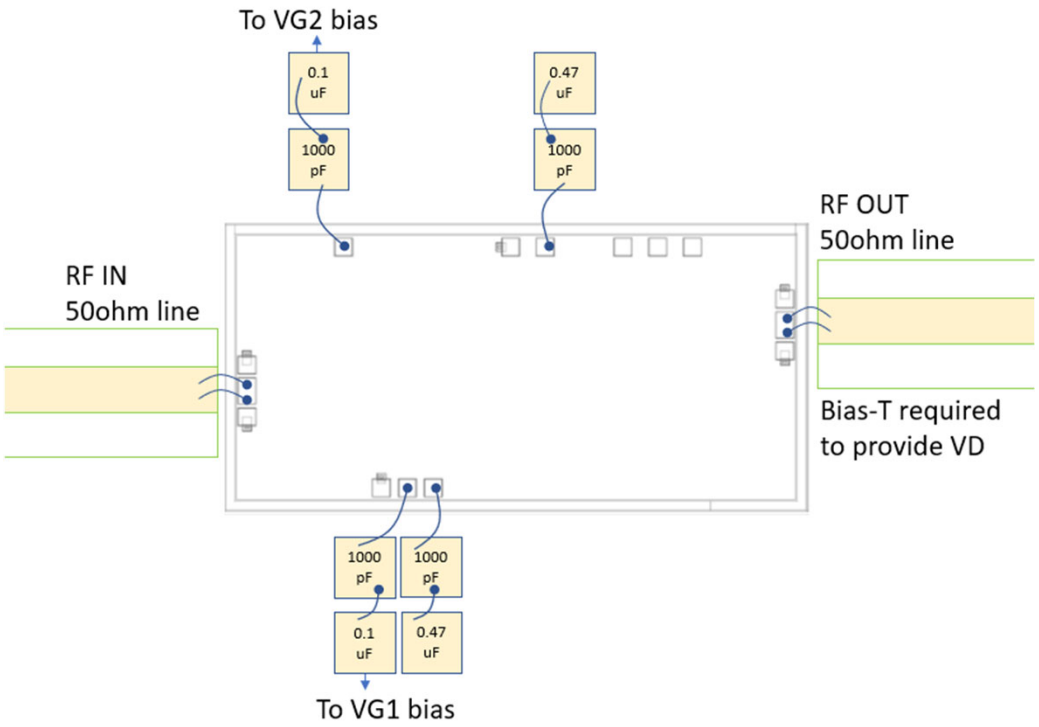
Power Detection: Vdet – Vref vs Pout at 40GHz, Vdiode = 1V



Power Detection: Vdet – Vref vs Frequency at P1dB, Vdiode = 1V



Assembly Drawing



Notes:

1. **Die thickness: 50um**
2. **DC bond pad is 100 x 100 µm²**
3. **RF IN/OUT bond pad is 100 x 160 µm²**
4. **Bond pad metalization: Gold**
5. **Backside metalization: Gold**
6. **Backside of the die (GND)**